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Molokai

Braswell CPU (TDP 6.5W) SoC

Project Information

Phase: DVT

POWER PLANE	VOLTAGE	CONTROL SIGNAL	Power States ACTIVE IN
+VIN	+19V		Always
VCCRTC	+1.5V		Always
+3V	+3.3V	MAIN_ON1	S0
+3V_S5	+3.3V	S5_LOAD_CODE	S0-S5
+3V_ALW	+3.3V	AC/DC Insert enable	Always (LDO)
+5V	+5V	MAIN_ON	S0
+5V_S5	+5V	S5_ON	S0-S5
+5V_ALW	+5V	AC/DC Insert enable	Always (LDO)
+3V_WLAN_P	+3.3V	WLAN_ON	S0-S5
+3V_LAN	+3.3V	LAN_PWR_ON	S0-S5
+1.35V_S3	+1.35V	S3_ON	S0-S3
+1.05V_S5	+2.5V	S5_ON	S0-S5
+1.8V_S5	+1.8V	S5_ON	S0-S5
+1.8V	+1.8V	MAIN_ON	S0
+VNN	+1.05V	S5_ON	S0-S5
+VGG	-	MAIN_ON	S0
CPU_CORE	-	VGG_PWRGD	S0
+1.8V_ALW	+1.8V	S5_ON	S0-S5
+1.15V_S5	+1.15V	S5_ON	S0-S5
+1.24V_S5	+1.24V	S5_ON	S0-S5
+0.65V_DDR_VTT	+0.675V	S3_ON	S3
+3V_S5_PRIME	+1V	S5_ON	S0-S5
+1.5V	+1.5V	MAIN_ON	S0

BOARD ID SETTING

	Board ID (Default = 00)	
Model	BOARD_ID1	BOARD_ID4
All EVT	0	0
All DVT	0	1
PVT1	1	0
PVT2+	1	1
MVB,A	0	0
1st Major ECN	0	1
2nd Major ECN	1	0
3rd Major ECN	1	1

	eMMC ID (Default = 00)			VRAM ID (Default = 00)				
eMMC	BOARD_ID5	BOARD_ID4	VRAM	BOARD_ID3	BOARD_ID2	BOARD_ID1	BOARD_ID6	
W/O	0	0	UMA	0	0			
Hynix	0	1	Hynix	0	1			
Samsung	1	0	Mircon	1	0			
Reserved	1	1	Reserved	1	1			

Schematic "Value" Definition

Molokai INTEL Platform		DB/SI/PV Stage				MP		
By Value format	Description	Auto BOM Control	Molokai	Lanai-U	Lanai-UE	Molokai	Lanai-U	Lanai-UE
XX	Install	V	V	V	V	V	V	V
*XX	Non-Install	V						
EV@XX	Install dGPU device	V	V			V		
SATA@XX	Install SATA device	V	V	V		V	V	
EMMC@XX	Install EMMC	V			V			V
PROTO@XX	Install in pre-production only	V	V	V	V			
MP@XX	Install in MP only	V				V	V	V

***Board ID by manual control

Molokai -2G : *

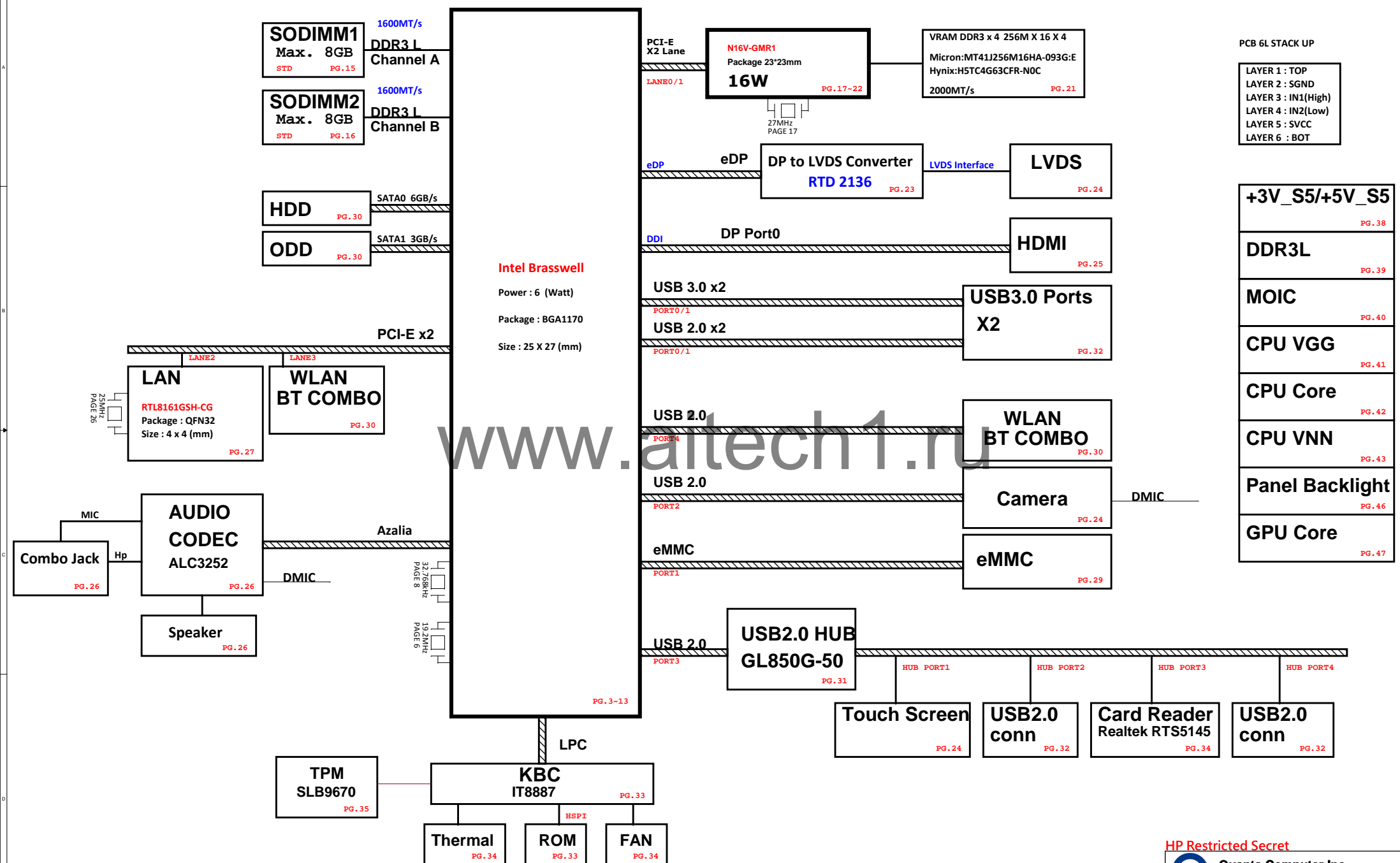
Molokai -UE : **

PCB AND SILKSCREEN COLOR

Program Phase	Color of PCB	Silkscreen
EVT	RED	YELLOW
DVT	LIGHT BLUE	YELLOW
PVT/MVB / PRODUCTION	GREEN	WHITE

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Molokai Intel Brasswell-M Platform Block Diagram



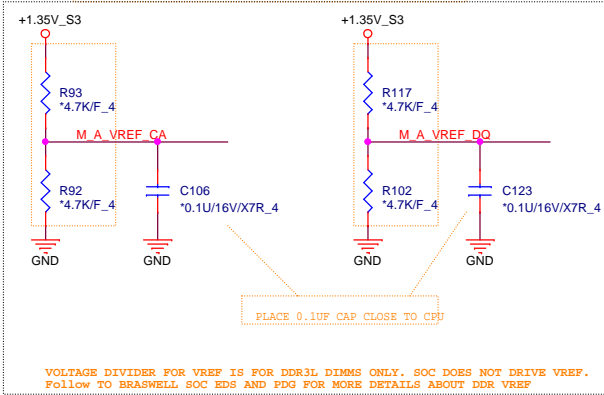
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Channel 0	Channel 1	SoC Supported Memory Operation Speed
1333 MHz	X	1066 MHz
1600 MHz	X	1600 MHz
1333 MHz	1333 MHz	1066 MHz
1600 MHz	1600 MHz	1600 MHz

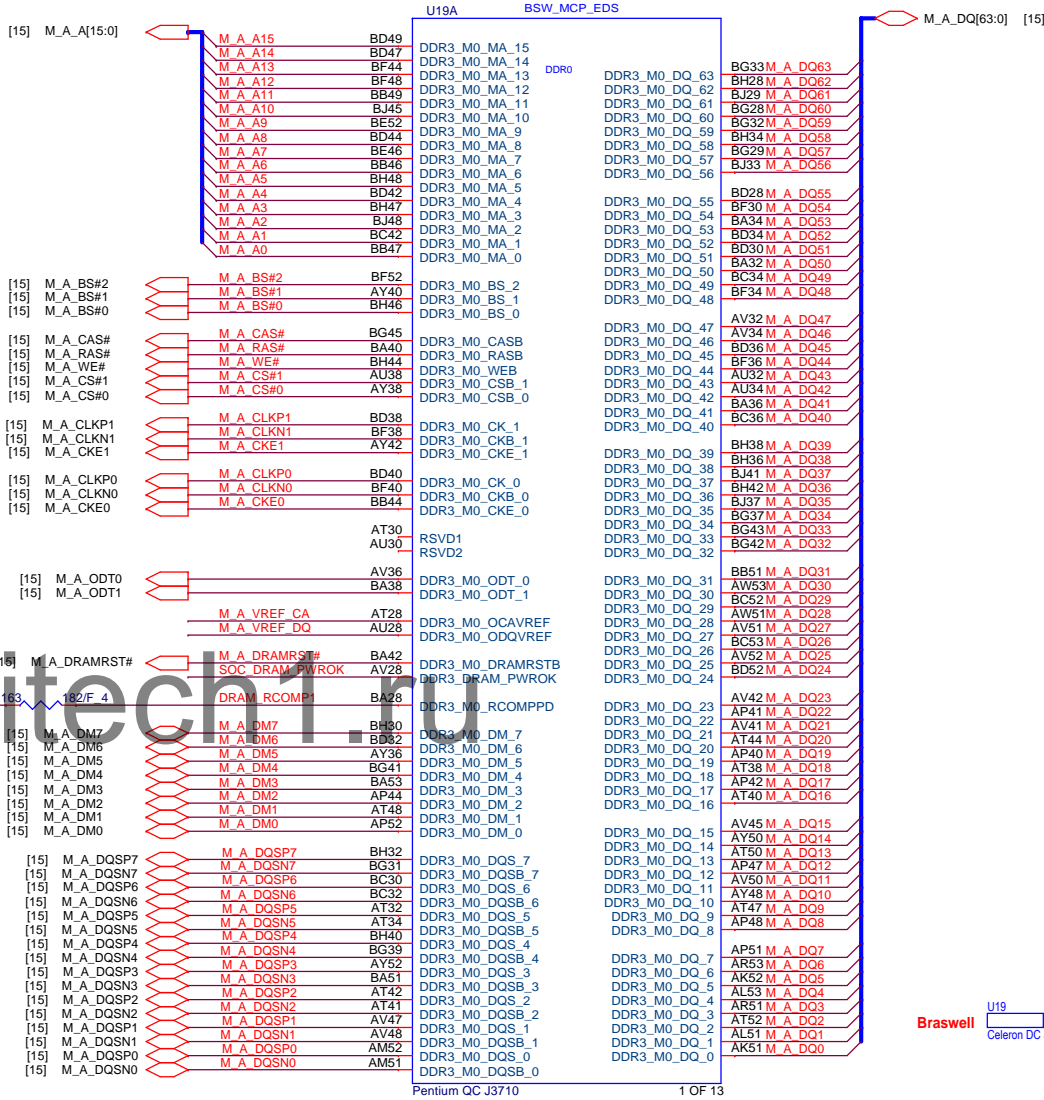
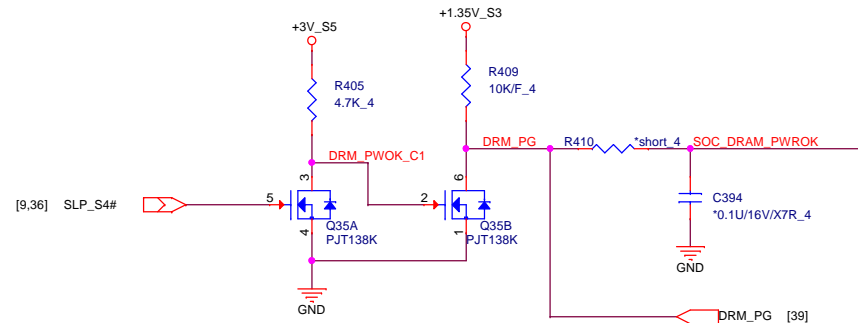
Channel 0 need to be populated first for the platform to power on

ROUTE ALL VREF POWER SIGNALS AS THICK TRACES

PLACE TWO 4.7K RESISTORS CLOSE TO CPU PINS ON M_VREF
ROUTE THE VREF POWER SIGNALS WITH THICK TRACES




VREF signals are not used for DDR3L designs.



[4,5,6,11,14,22,24,27,30,31,32,33,35,36,37,38,40,41,42,43,44,48] +1.35V_S3 +3V_S5

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PROJECT: HP-Molokai

Size Custom

Document Number

Braswell (DDRA)

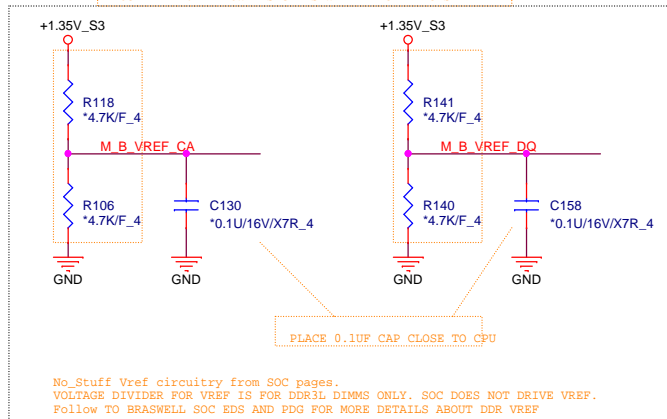
Rev 1A

Date: Monday, January 18, 2016

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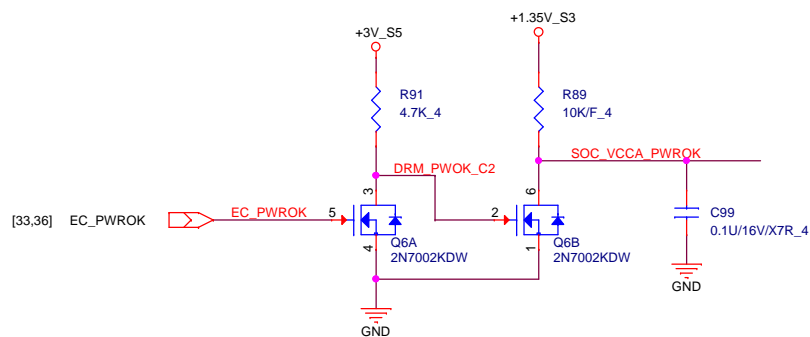
ROUTE ALL VREF POWER SIGNALS AS THICK TRACES

PLACE TWO 4.7K RESISTORS CLOSE TO CPU PINS ON M_VREF
ROUTE THE VREF POWER SIGNALS WITH THICK TRACES

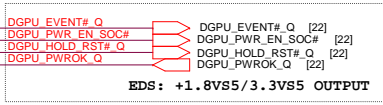
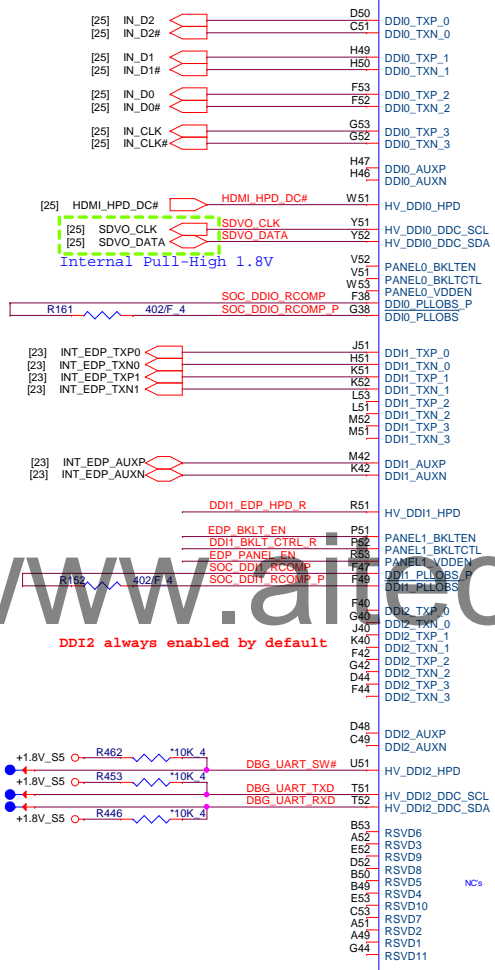


VREF signals are not used for
DDR3L designs.

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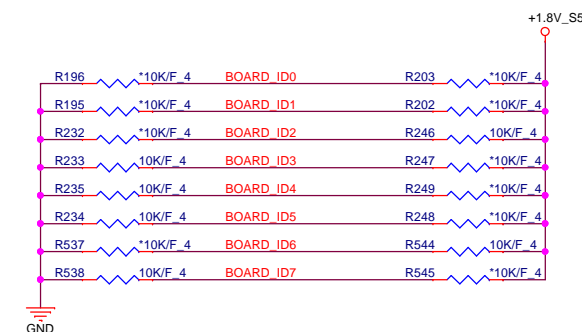
[3,5,6,11,14,22,24,27,30,31,32,33,35,36,37,38,40,41,42,43,44,48] +1.35V_S3
[3,11,15,16,39] +3V_S5



	Board ID (Default = 00)	
Model	BOARD_ID7	BOARD_ID6
EC-SI-03		
All EVT	0	0
All DVT	0	1
PVT1	1	0
PVT2+	1	1
MVB,A	0	0
1st Major ECN	0	1
2nd Major ECN	1	0
3rd Major ECN	1	1

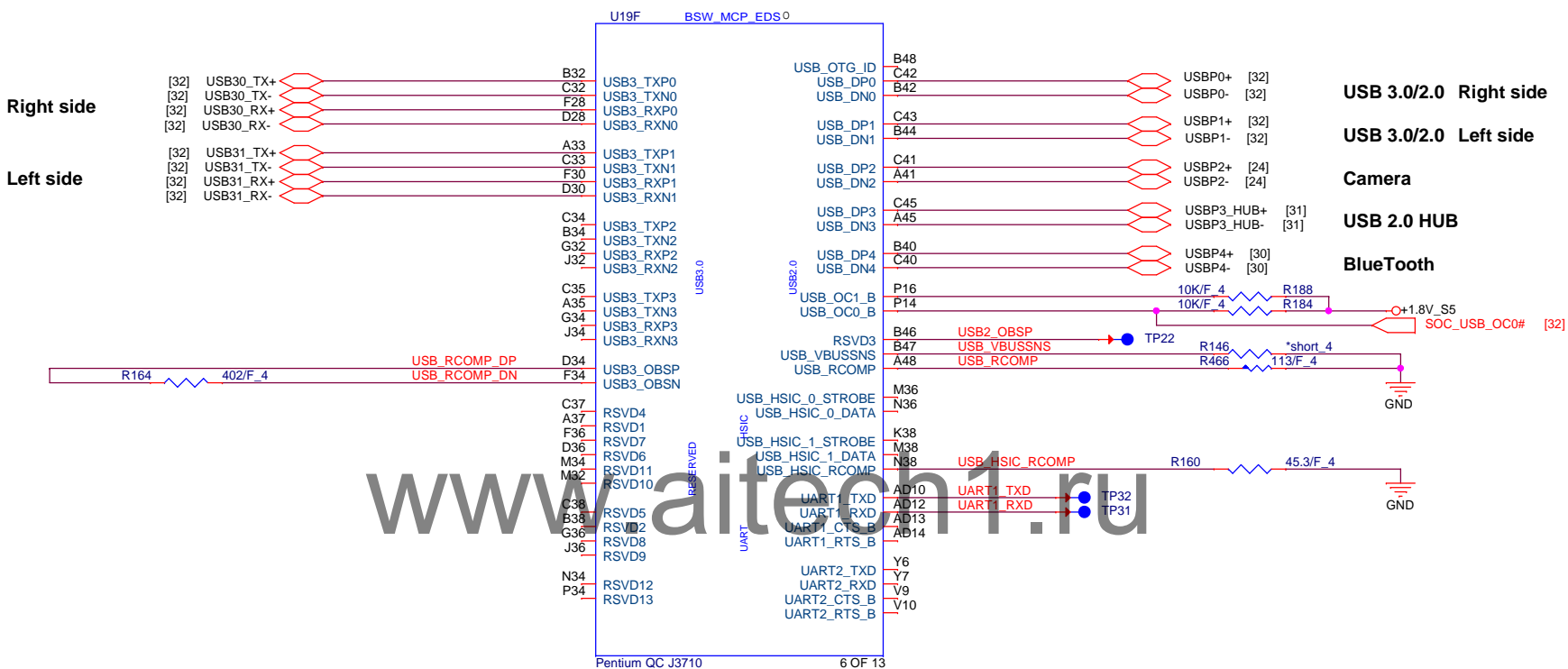
	Board ID (Default = 00)	
eMMC	BOARD_ID5	BOARD_ID4
W/O	0	0
Hynix	0	1
Samsung	1	0
Reserved	1	1

	Board ID (Default = 00)			
VRAM	BOARD_ID3	BOARD_ID2	BOARD_ID1	BOARD_ID0
UMA	0	0		
Hynix	0	1		
Mircon	1	0		
Reserved	1	1		



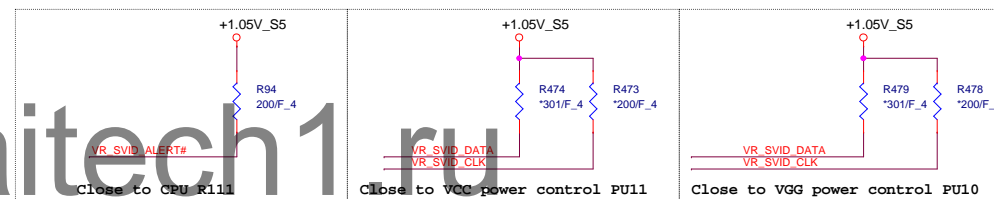
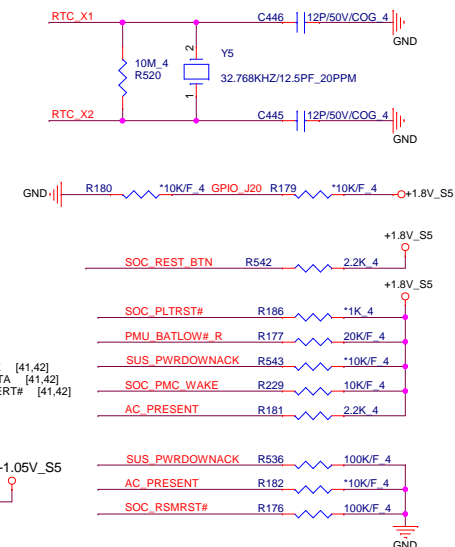
 **Quanta Computer Inc.**
PROJECT: HP-Molokai

Size Custom	Document Number Braswell (I2C/GPIO/CLK)	Rev 2A
Date:	Monday, January 18, 2016	Sheet 7 of 54

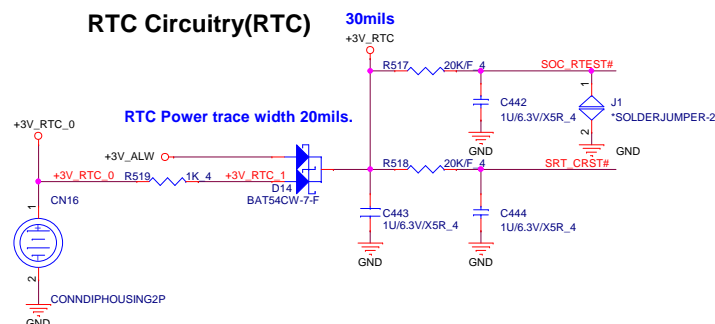


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		PROJECT: HP-Molokai	
Size Custom	Document Number Braswell (USB/URAT)	Date: Monday, January 18, 2016	Rev 1A
Sheet 8 of 54		1	



RTC Circuitry(RTC)



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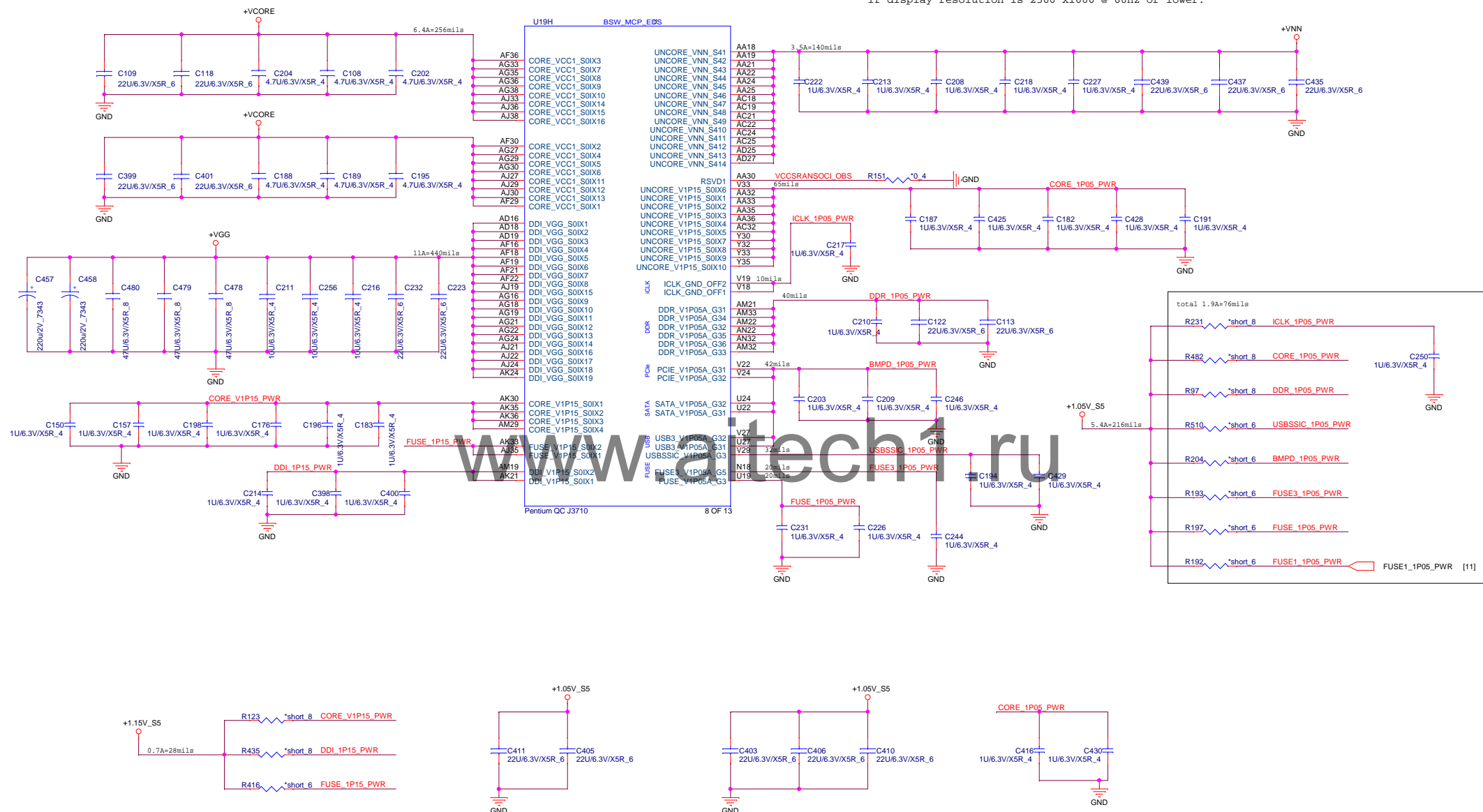


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Size Custom	Document Number Braswell (RTC/LPC/PMU)	Rev 1A
Date: Monday, January 18, 2016	Sheet 9 of 54	

VNN can optionally be merged with V1P05A
if display resolution is 2560 x1600 @ 60Hz or lower.



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Size
Custom

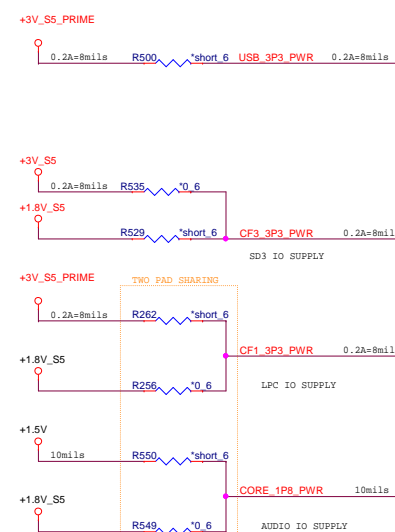
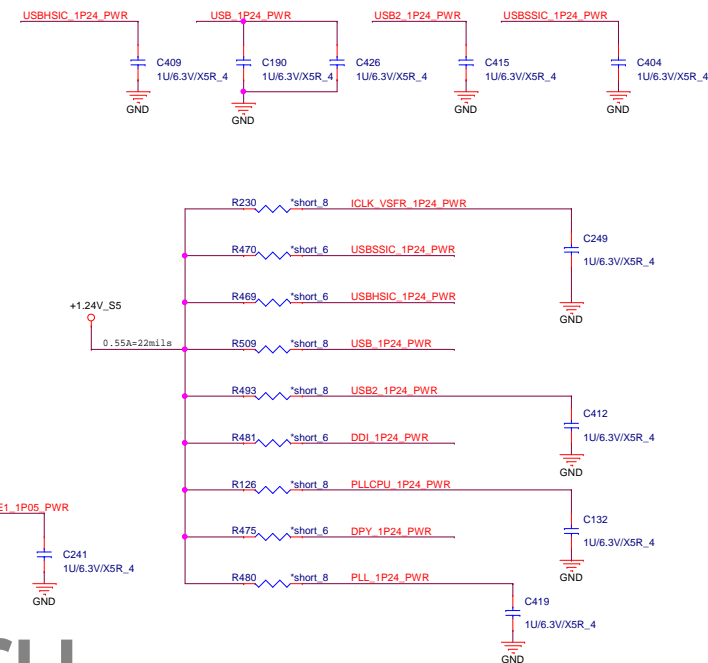
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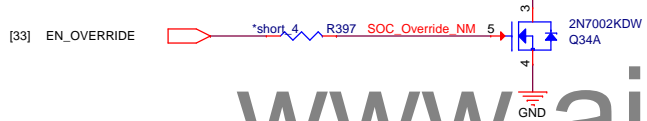
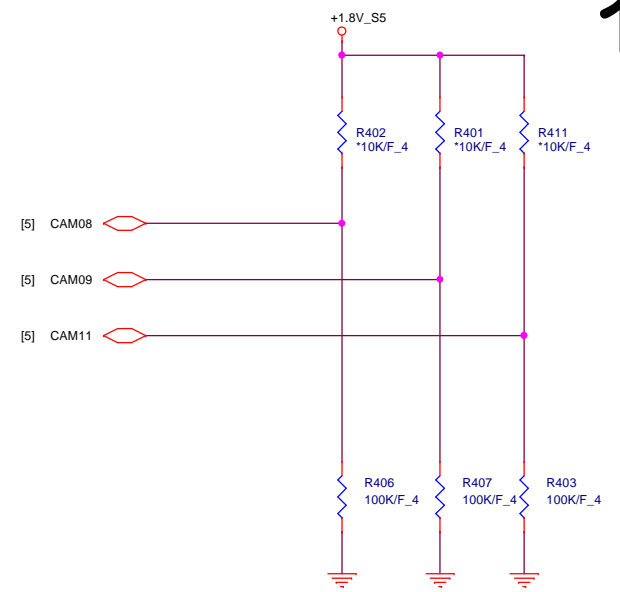
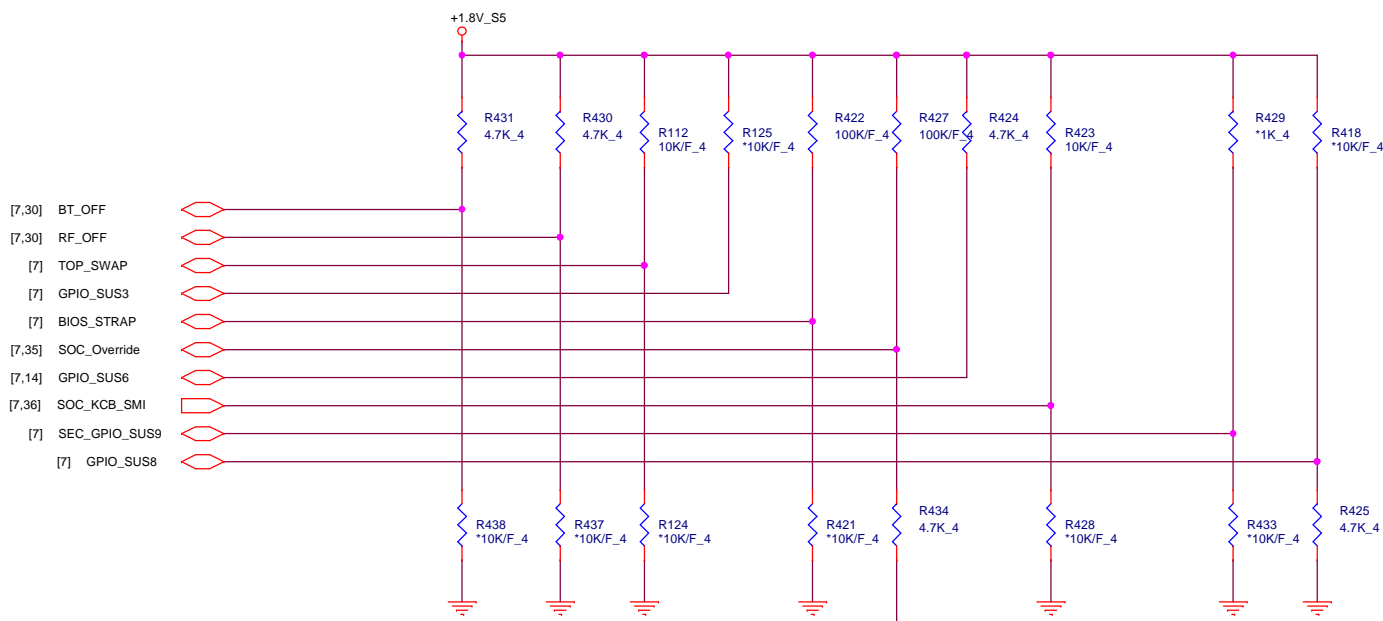
Braswell (Power 1)

Rev	1A
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REQUIRED STRAPS

	GPIO_SUS0	GPIO_SUS1	TOP_SWAP	GPIO_SUS3	BIOS_STRAP	SOC_Override	GPIO_SUS6	SOC_KCB_SMI	GPIO_SUS8
PULL HIGH	DDI0 detected DEFAULT	DDI1 detected DEFAULT	Normal Operation DEFAULT	Reserve 10 KΩ PU DEFAULT	SPI DEFAULT	Normal Operation DEFAULT 20150209 PV change	10 KΩ PU to 1.8V DEFAULT	Reserve 10 KΩ PU DEFAULT	Supply is 1.35V
PULL LOW	DDI0 not detected	DDI1 not detected	Change Boot Loader address		LPC	Override			Supply is 1.25V DEFAULT

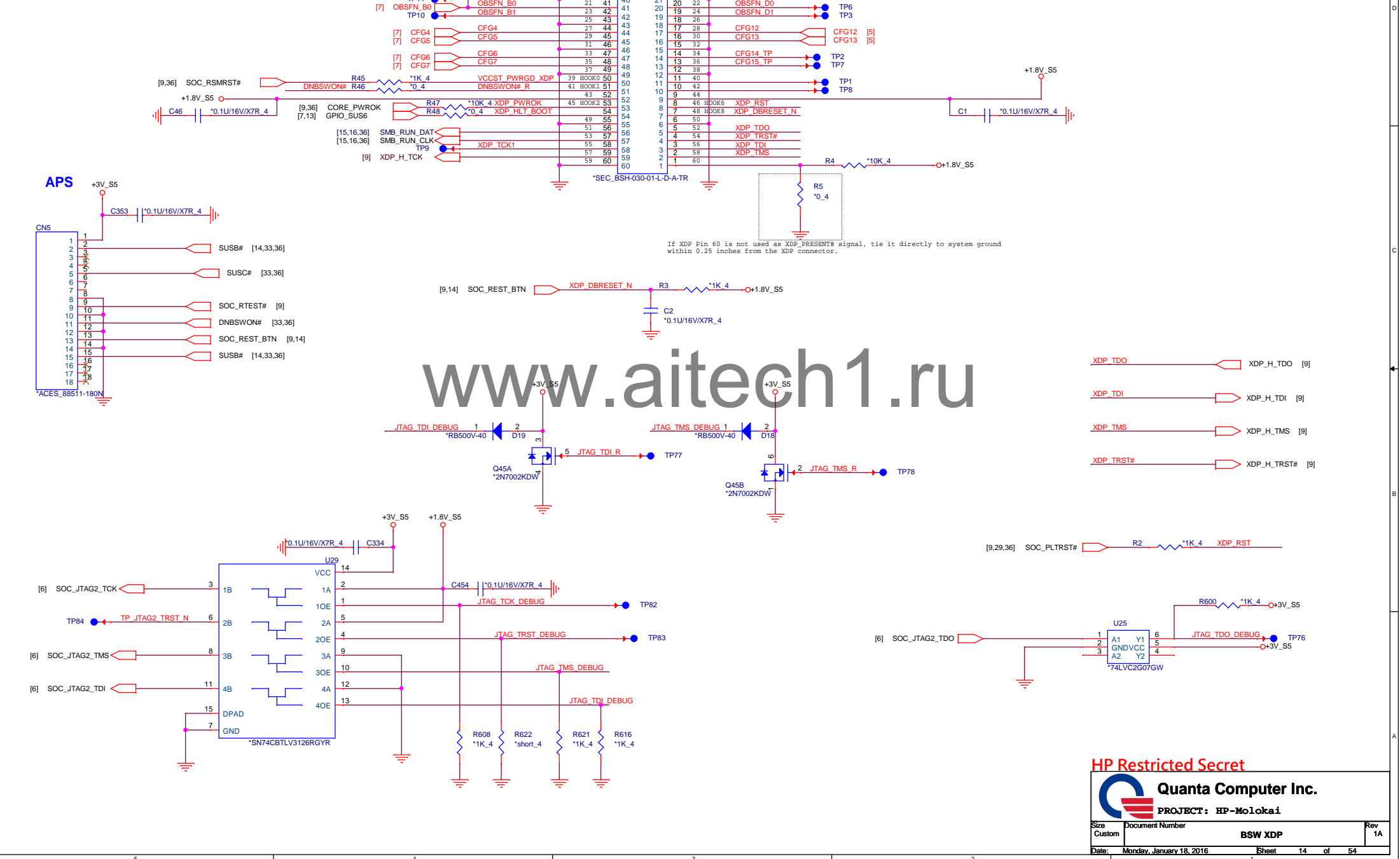
	CAM08	CAM09	CAM11
PULL HIGH	ICLK Xtal OSC Bypass	CCU SUS RO Bypass	RTC OSC Bypass
PULL LOW	ICLK Xtal OSC No Bypass DEFAULT	CCU SUS RO No Bypass DEFAULT	RTC OSC No Bypass DEFAULT

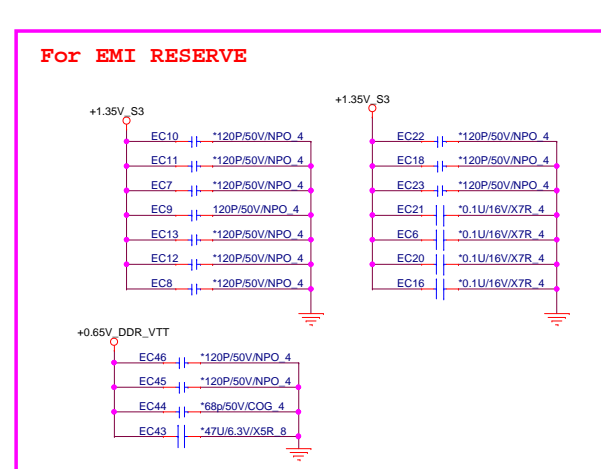
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PROJECT: HP-Molokai

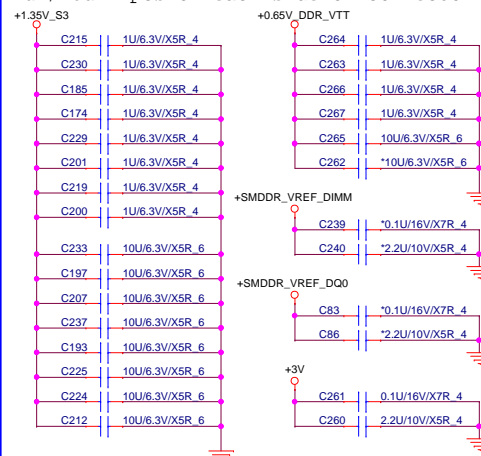
Size Custom	Document Number	Braswell (Strap)	Rev 1A
Date: Monday, January 18, 2016	Sheet 13	of 54	



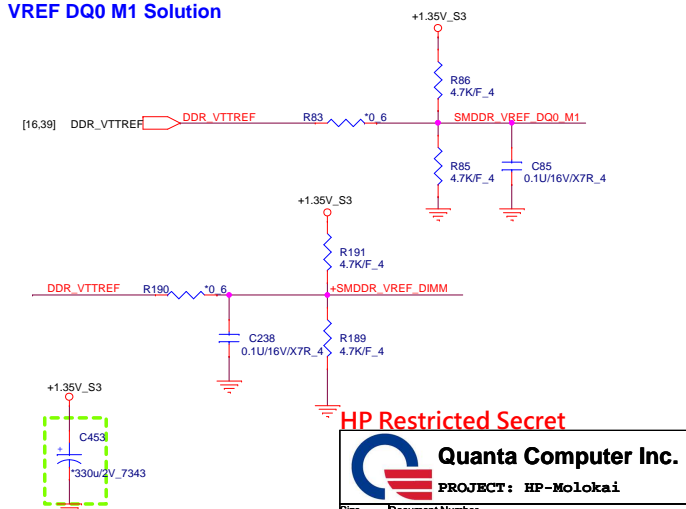


Place these Caps near So-Dimm0.

1uF/10uF 4pcs on each side of connector



VREF DQ0 M1 Solution



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PROJECT: HP-Molokai

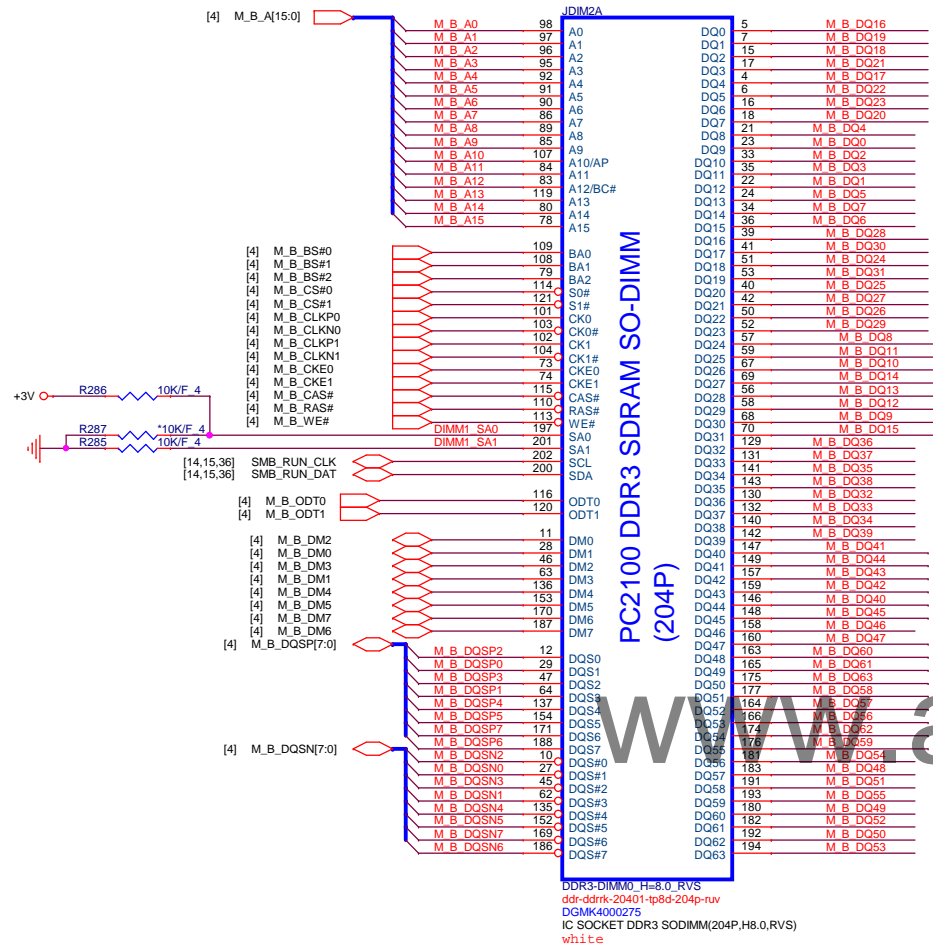
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Business Number

DDR3L DIMM0-RVS(8.0H)

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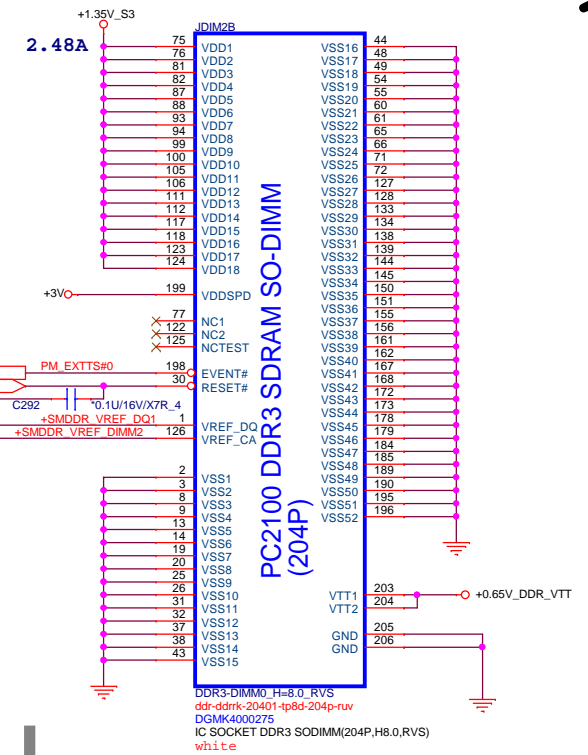
M_B_DQ[63:0] [4]



SMDDR_VREF_DQ1_M1

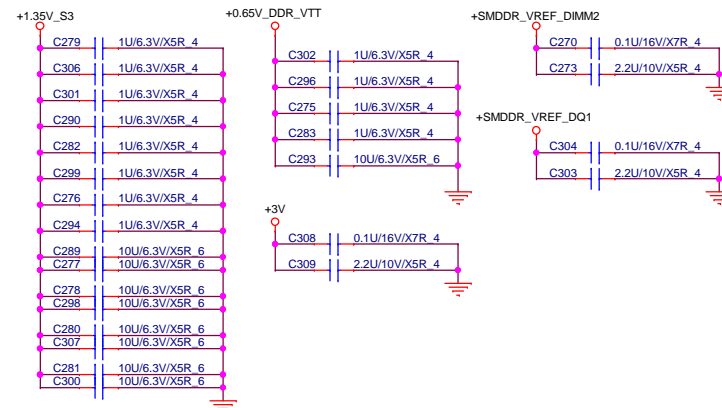
[15] PM_EXTTS#0

[4] M_B_DRAMRST#

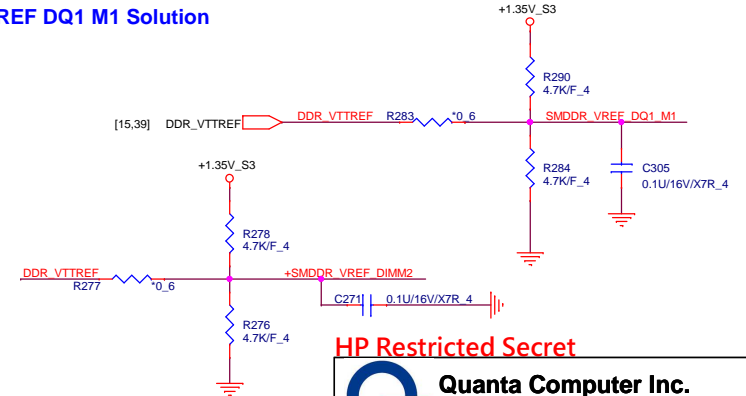


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Place these Caps near So-Dimm1.
1uF/10uF 4pcs on each side of connector



VREF DQ1 M1 Solution



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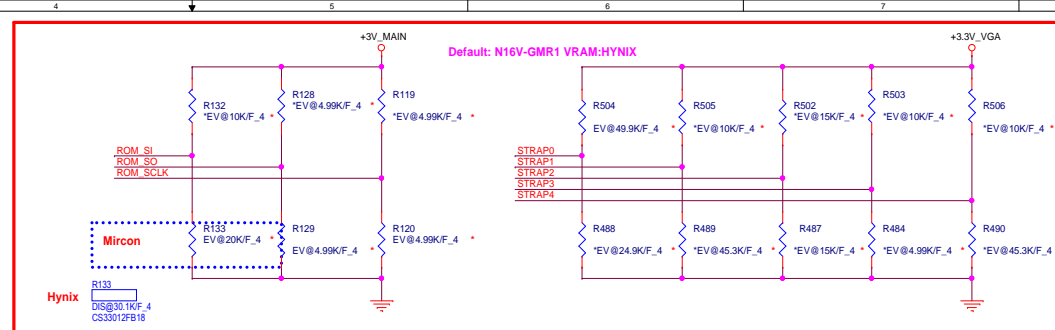
PROJECT: HP-Molokai

Size: Custom
Document Number: DDR3L DIMM1-RVS(8.0H)
Date: Monday, January 18, 2016
Sheet: 16 of 54
Rev: 1A









```

ROM_SCLK = Stuff 4.99K pull down
ROM_SO   = Stuff 4.99K pull down
STRAP0   = Stuff 49.9K pull up
STRAP1   = NC
STRAP2   = NC
STRAP3   = NC
STRAP4   = NC
ROM_SI   = VRAM Configuration follow below table

```



```

ROM_SCLK = Stuff 4.99K pull up
ROM_SO   = Stuff 4.99K pull up.
STRAP0   = Stuff 45.3k pull up. (EDID Panel)
STRAP1   = Stuff 4.99k pull down.(Gen3 support)
STRAP2   = Stuff 10k pull up.(DID 0x1299)
STRAP3   = Stuff 4.99k pull down.(No display out)
STRAP4   = Stuff 45.3k pull down. (Gen3/max speed)
ROM_SI   = VRAM Configuration follow below table

```



```

ROM_SCLK = Stuff 4.99K pull up
ROM_SO   = Stuff 4.99K pull up.
STRAP0   = Stuff 45.3k pull up. (EDID Panel)
STRAP1   = Stuff 4.99k pull down.(Gen3 support)
STRAP2   = Stuff 15k pull up.(DID 0x129A)
STRAP3   = Stuff 4.99k pull down.(No display out)
STRAP4   = Stuff 45.3k pull down. (Gen3/max speed)
ROM_SI   = VRAM Configuration follow below table

```

Note: GC6 2.0 is supported by N16x GPU in the GB2B, GB4B-128, and GB3B-256 packages.

Logical Strap Bit Mapping

Logic	PU-VDD	PD	QCI P/N
4.99K	1000	0000	CS24992FB2
10K	1001	0001	CS31002FB2
15K	1010	0010	CS31502FB2
20K	1011	0011	CS32002FB2
24.9K	1100	0100	CS32492FB1
30.1K	1101	0101	CS33012FB1
34.8K	1110	0110	CS33482FB1
45.3K	1111	0111	CS34532FB1

GPIO ASSIGNMENTS

GPI/O	I/O	PIN	USAGE
0	IN	FB_CLAMP_MON	FB Clamp monitor (GC6 1.0)
0	OUT	GC6_FB_EN	GC6 FB Enable (GC6 2.0)
5	OUT	+3V_MAIN_EN	Enable GC6 +3V_MAIN
6	OUT	FB_CLAMP_REQ#	Active low FB Clamp toggle request (GC6 1.0)
6	IN	DGPU_EVENT#	DGPU EVENT from CPU (GC6 2.0)
8	OUT	VGA_OVT#	ACTIVE LOW THERMAL OVER TEMP
9	OUT	ALERT	ACTIVE LOW THERMAL ALERT
11	OUT	PWR_VID	GPU CORE_VDD PWM Control signal
12	IN	PWR_LEVEL	AC Power detect or power supply overdraw input
13	OUT	PSI	Phase Shedding

N16S-GM/-GT/-LP VRAM Configuration Table

[illegible]

N16V-GM/GL VRAM Configuration Table

HWT-CM3E1 RAM Configuration Table				ROM_S1				
RAMCFG [3:0]	DESCRIPTION	1.5V DDR3	Vendor	Vendor P/N	ROM_S1	STN_B/S	Configuration	
	256Mx16							
0001	DDR3L 256Mx16, 64bit, 4Gb, 1000MHz		Micron	MT412J256M16HA-093G:E	PD 10k ohm	AKD5PZSTL05	Single Rank or Single Rank stuffing for Dual Rank	
0010	DDR3L 256Mx16, 64bit, 4Gb, 1000MHz		HYNIX	H5TC4G63AFR-11C	PD 15K ohm	AKD5PGWTW13		
0100	DDR3L 256Mx16, 64bit, 4Gb, 1000MHz		SAMSUNG	K4W4G1644D-BCL1	PD 24.9K ohm	AKD5PGWT504		
1001	DDR3L 256Mx16, 64bit, 4Gb, 1000MHz		HYNIX	H5TC4G63CFR-N0C	PU 10K ohm	AKD5PZDTW03		

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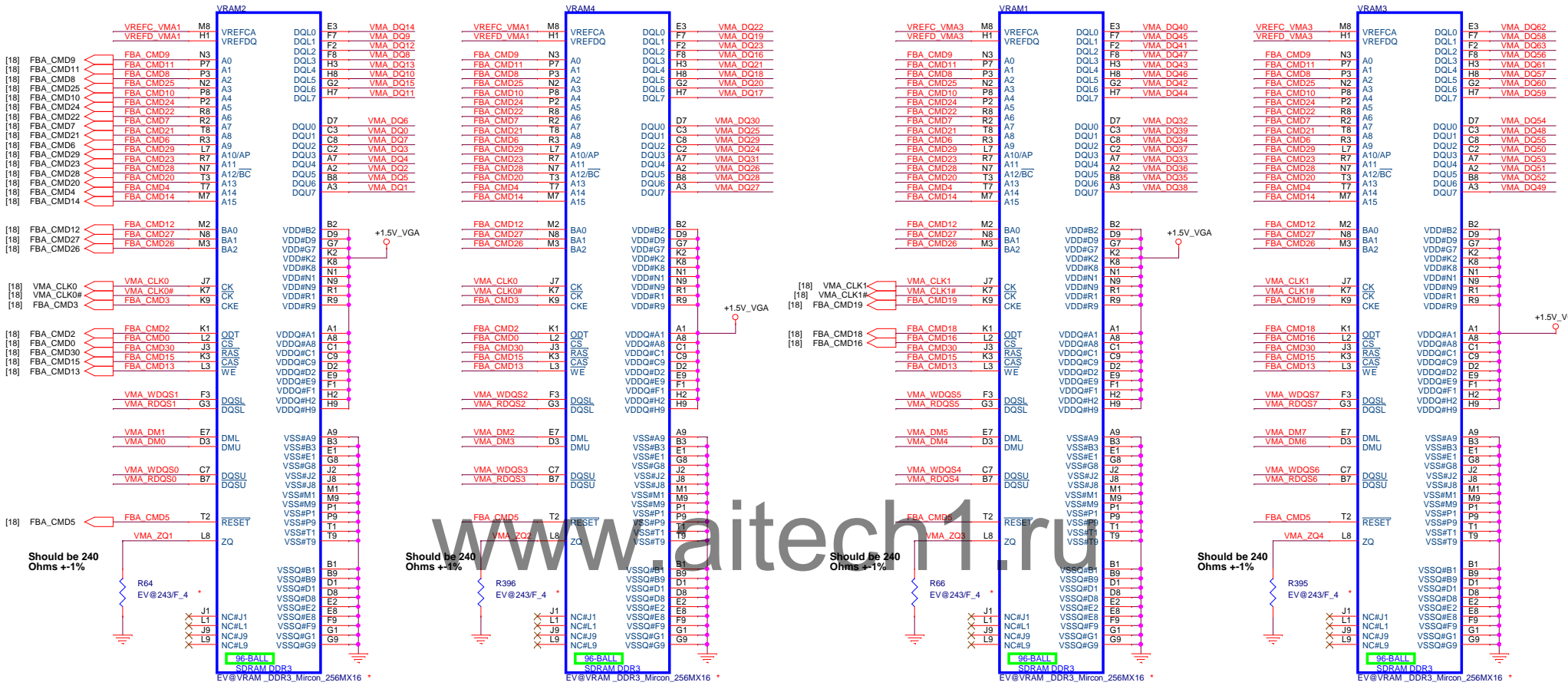
Size	Document Number	Rev
	N16V-GMR (GPIO/STRAPS)	2A
Date:	Monday, January 18, 2016	Sheet 20 of 54

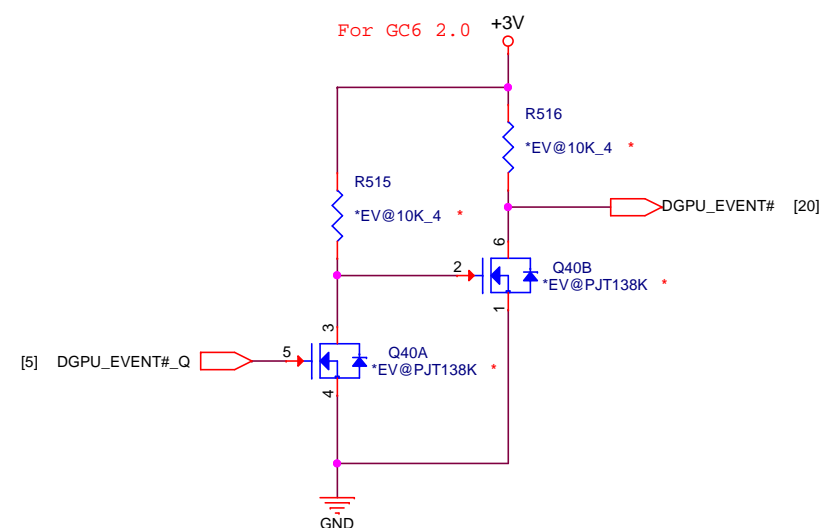
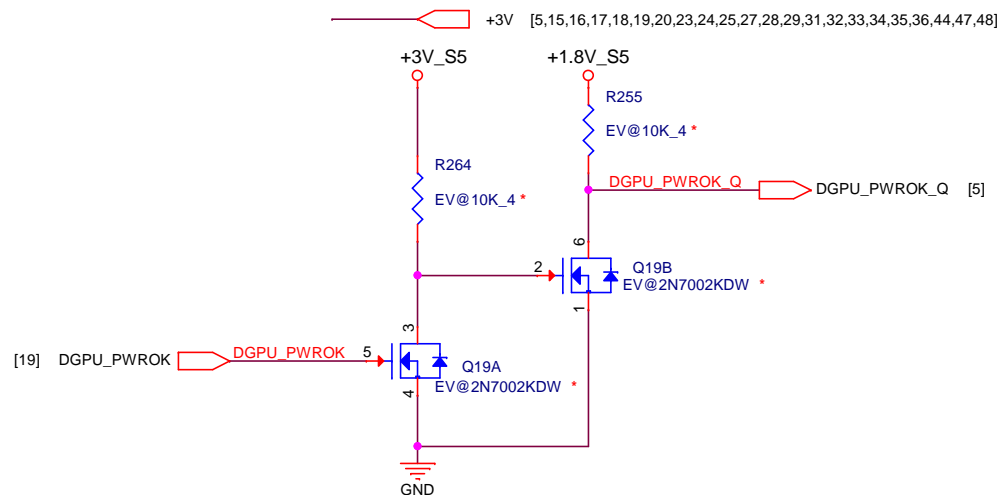
CHANNEL A: 2048MB DDR3X16

+1.05V_VGA [17,18,19,48]
+1.5V_VGA [18,48]

HYU 256Mx16, HSTC4G63AFR-11C STN B/S PN : AKD5PGWTW13
MIC 256Mx16, MT41J256M16HA-093G:E STN B/S PN : AKD5P2STL05
SAM 256Mx16, K4W4G1646D-BC1A STN B/S PN : AKD5PGWT504

[18] VMA_DQ[63:0]
[18] VMA_DM[7:0]
[18] VMA_WDQS[7:0]
[18] VMA_RDQS[7:0]





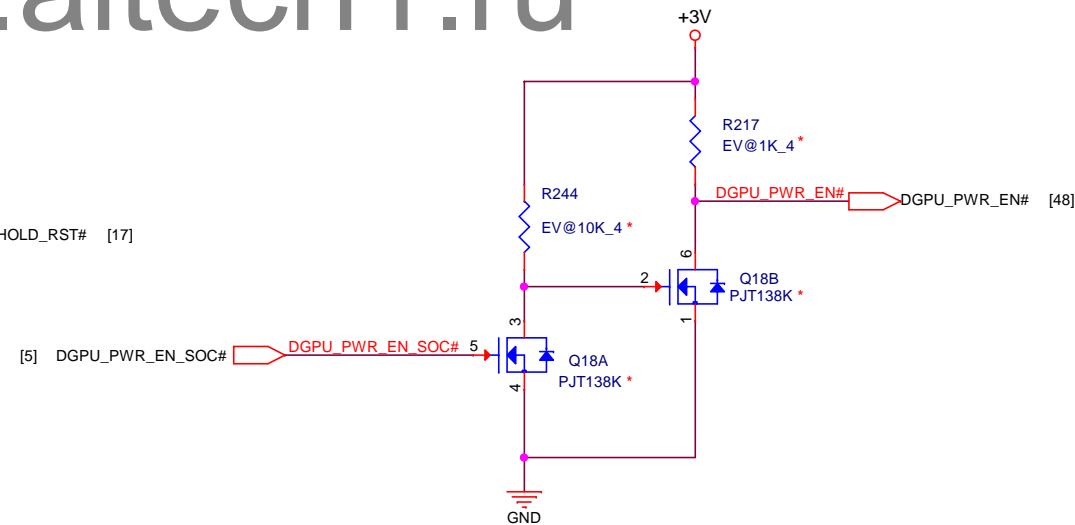
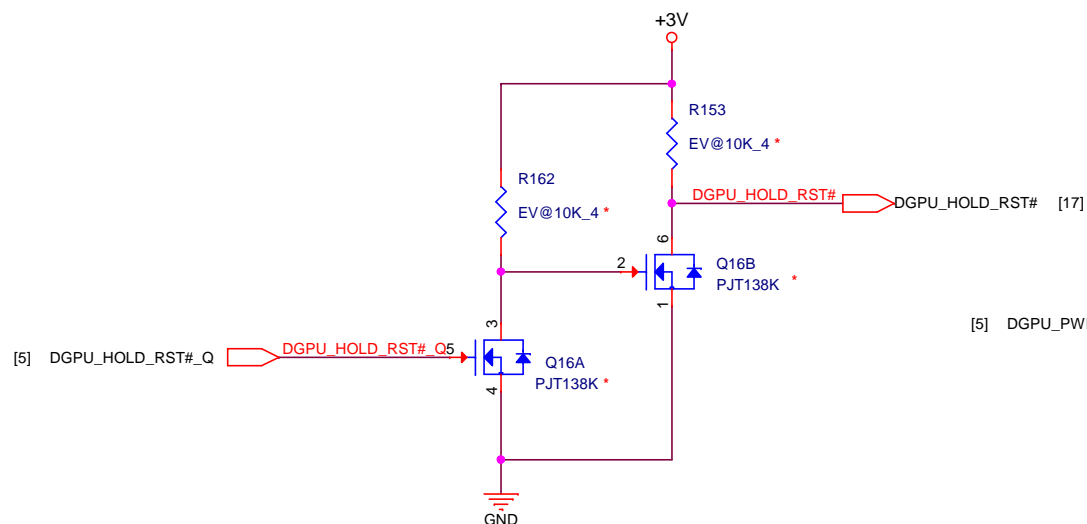
DGPU_PWROK R257 *EV@0_4* DGPU_PWROK_Q

DGPU_EVENT# Q R514 *EV@0_4* DGPU_EVENT#


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DGPU_PWR_EN_SOC# R223 *EV@0_4* DGPU_PWR_EN#

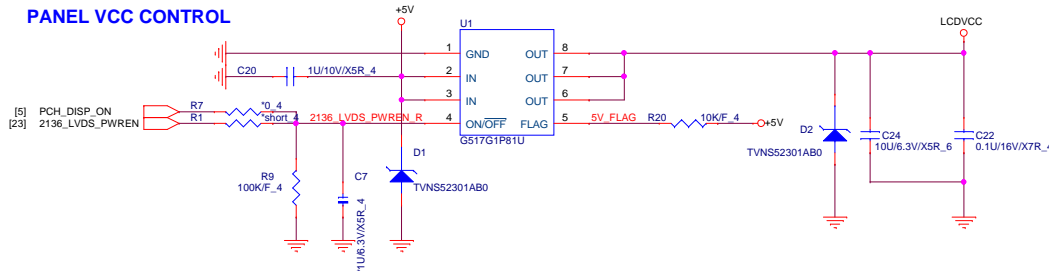
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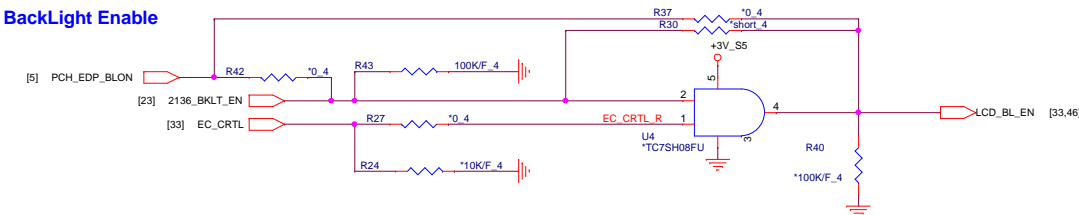
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 Quanta Computer Inc. PROJECT: HP-Molokai		Rev
		1A
Size	Document Number	
dGPU Level Shift		
Date:	Monday, January 18, 2016	Sheet 22 of 54

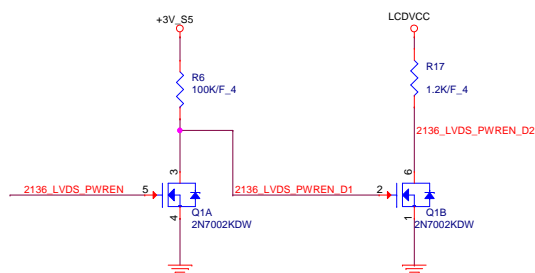
PANEL VCC CONTROL



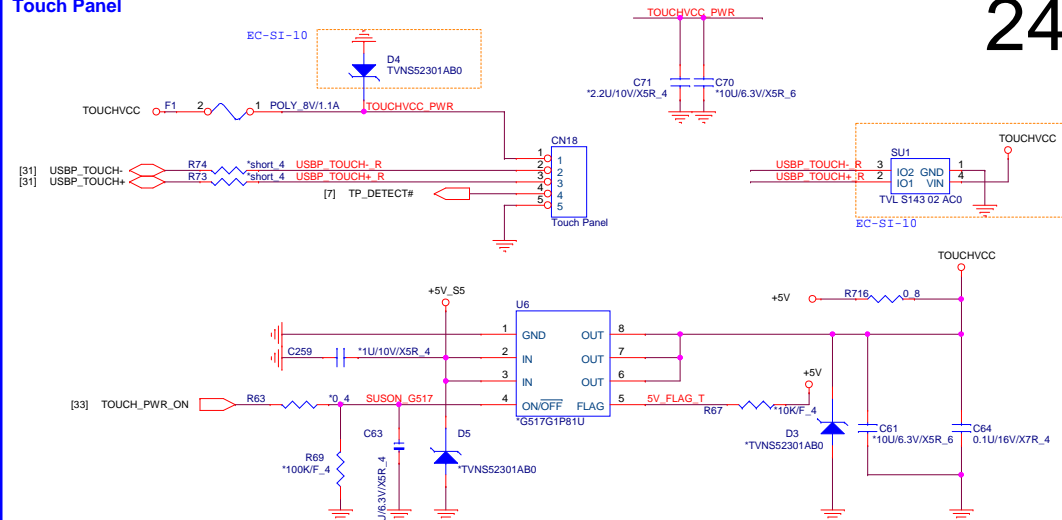
BackLight Enable



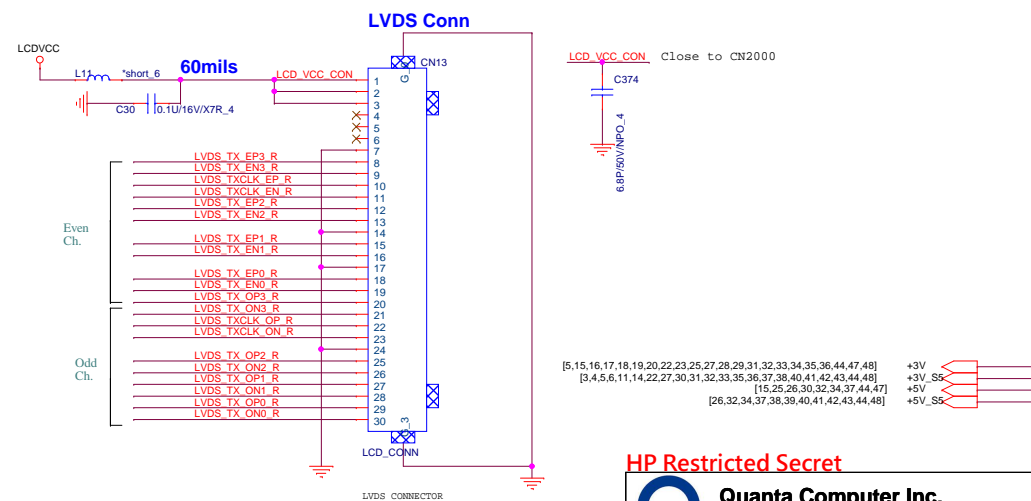
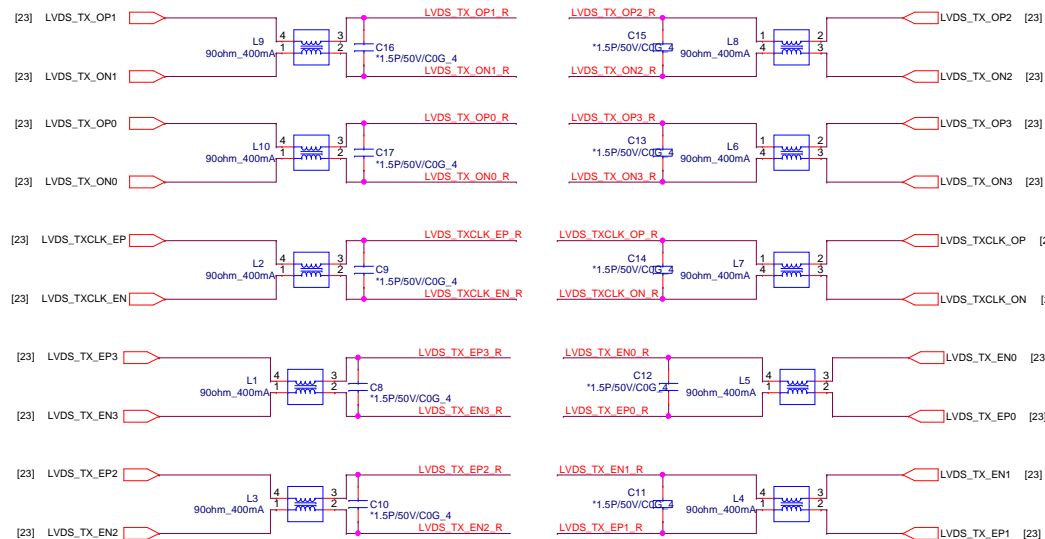
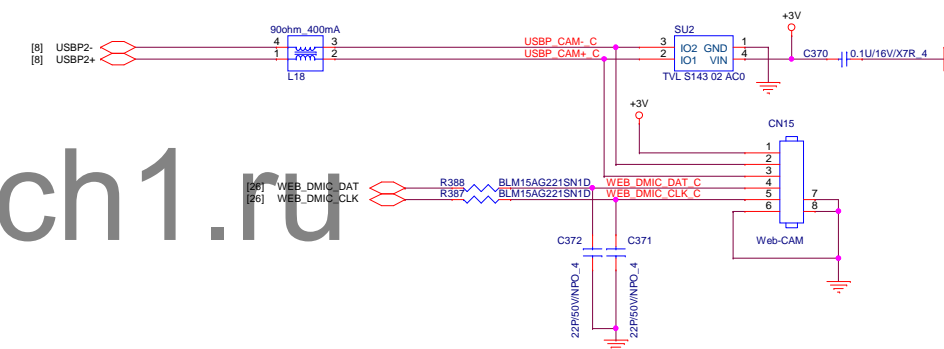
LCDVCC Discharge Circuit



Touch Panel



CCD CONN



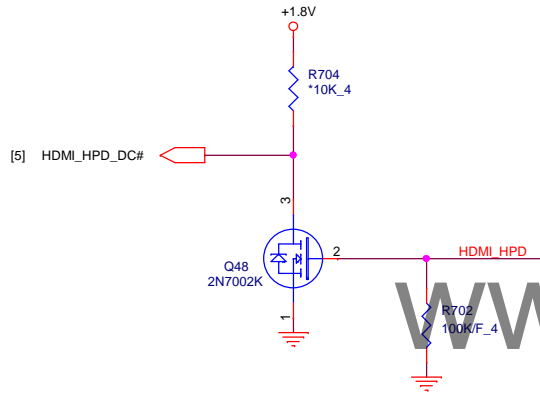
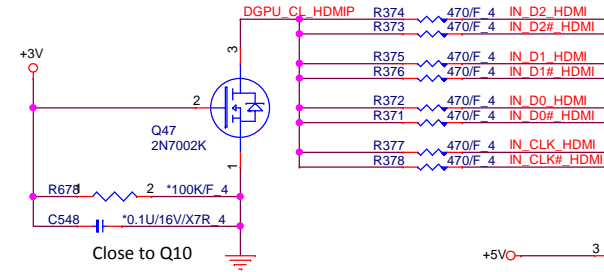
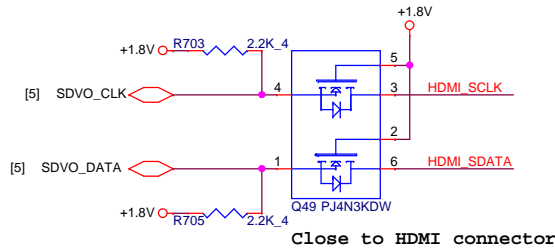
HP Restricted Secret

Quanta Computer Inc.
PROJECT: HP-Molokai

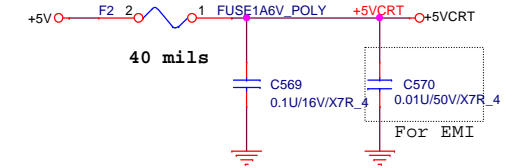
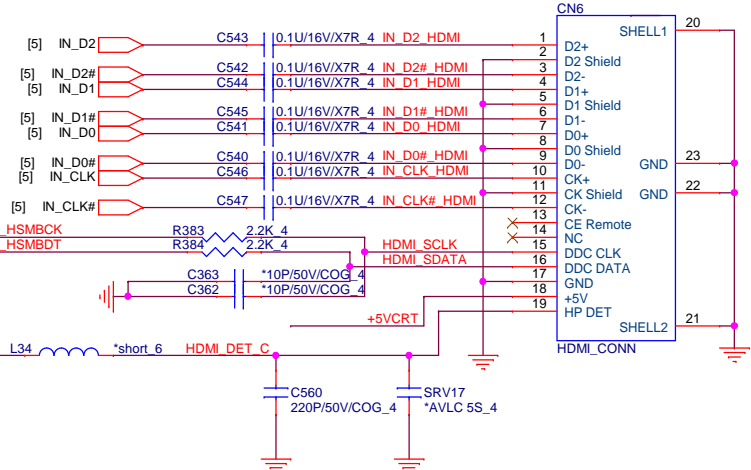
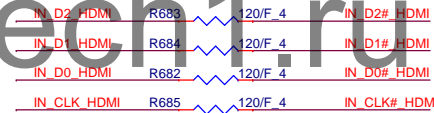
Size Custom Document Number LCD CONN/CCD/TouchPanel Rev 2A
Date: Monday, January 25, 2016 Sheet 24 of 54

HDMI CONN

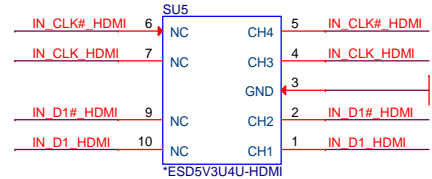
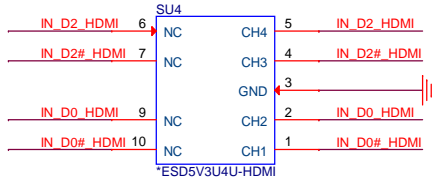
25



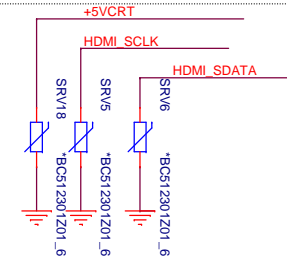
For EMI



For ESD



Layout note: Place close to HDMI Conn



[5,6,27,29,30,34,36,40]
[5,15,16,17,18,19,20,22,23,24,27,28,29,31,32,33,34,35,36,44,47,48]
[15,24,26,30,32,34,37,44,47]

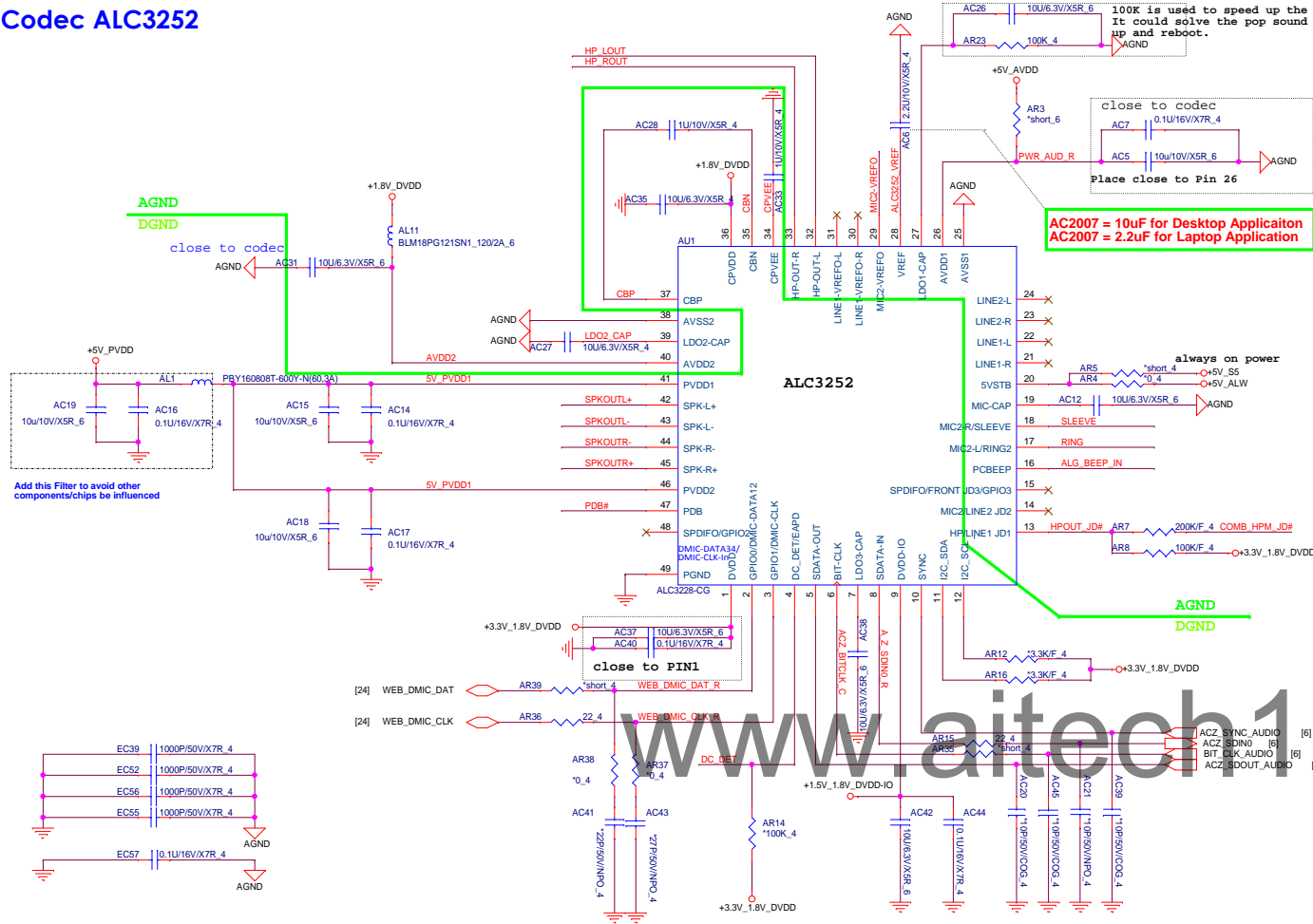
+1.8V
+3V
+5V

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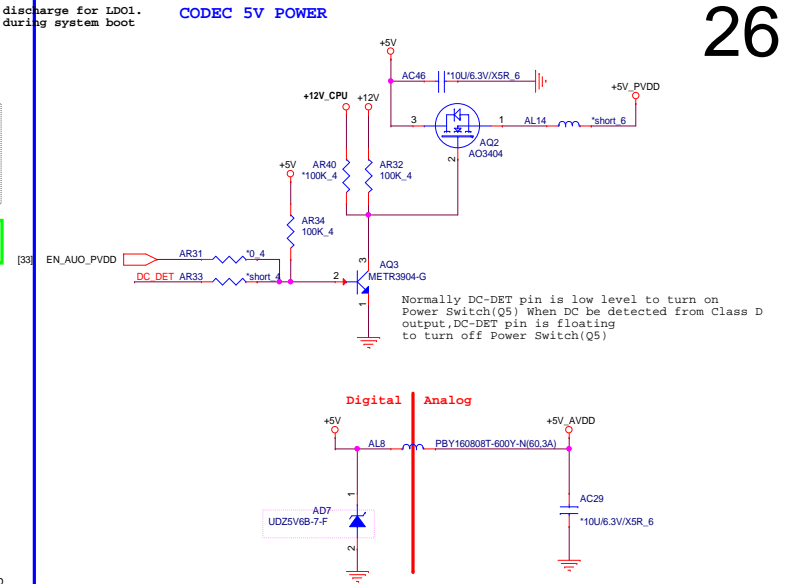
Quanta Computer Inc.
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Size	Document Number	Rev
Custom	HDMI	1A

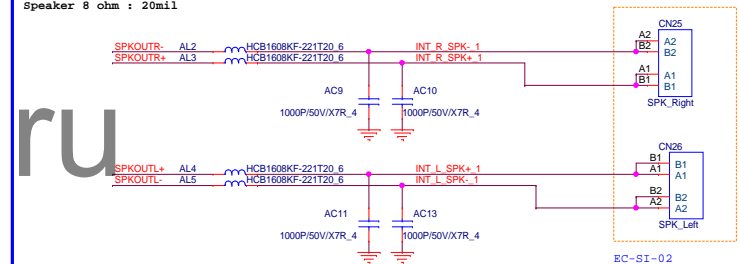
Date: Monday, January 18, 2016 Sheet 25 of 54



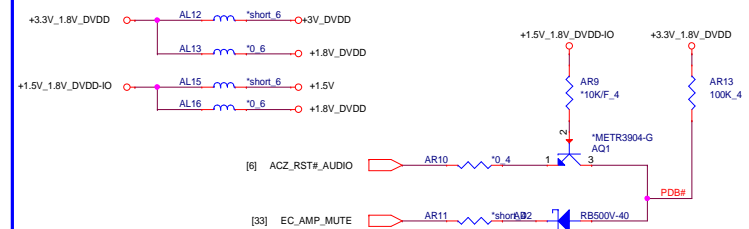
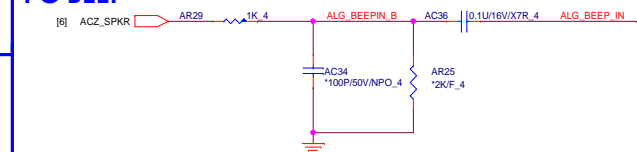
CODEC 5V POWER



Trace width for SPK-L+/SPK-L-/SPK-R+/SPK-R-Speaker
4 ohm : 40mil
Speaker 8 ohm : 20mil



PC BEEP



If the voltage level of MHPDA_RESET# is 1.8V, that means the Mobile HDA_Link run at 1.8V level, please add a level shift circuit(Q7/R84).

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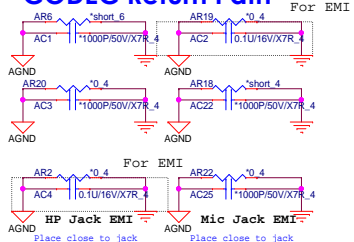


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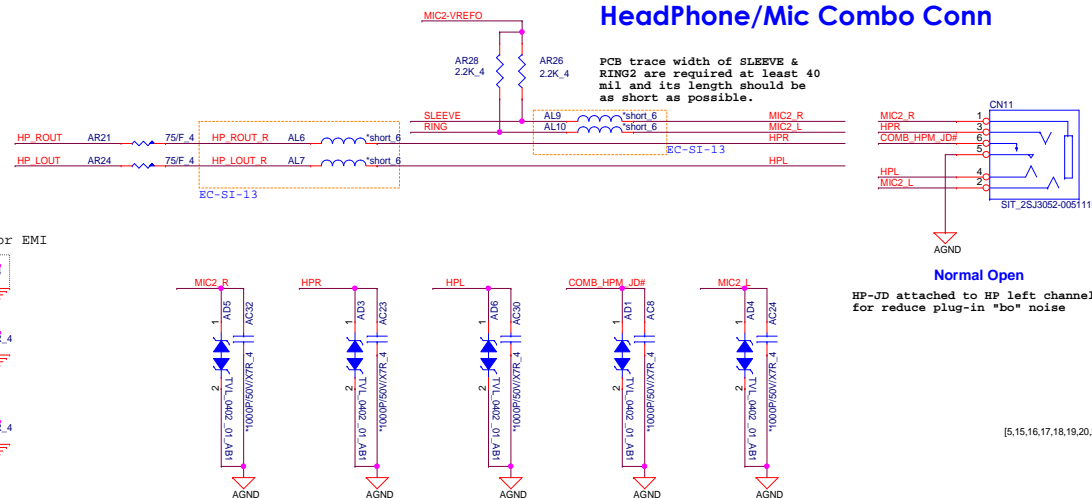
PROJECT: HP-Molokai

Size Custom	Document Number Audio Codec(ALC3252)
Date: Monday, January 18, 2016	Sheet 26 of 54

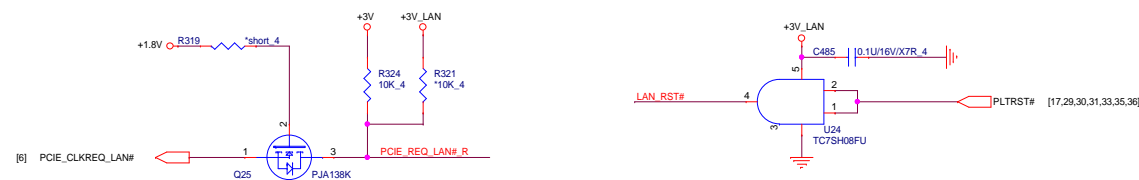
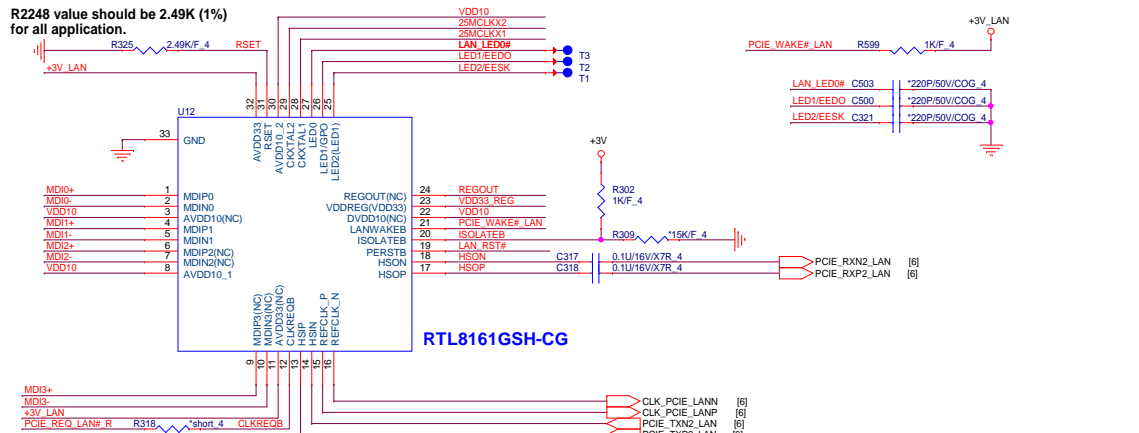
CODEC Return Path



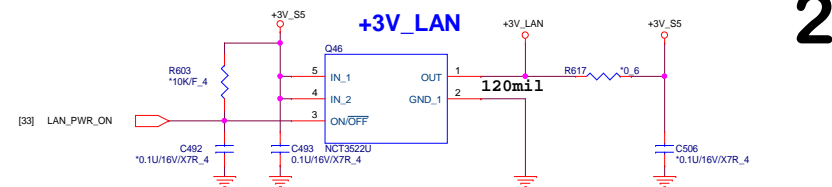
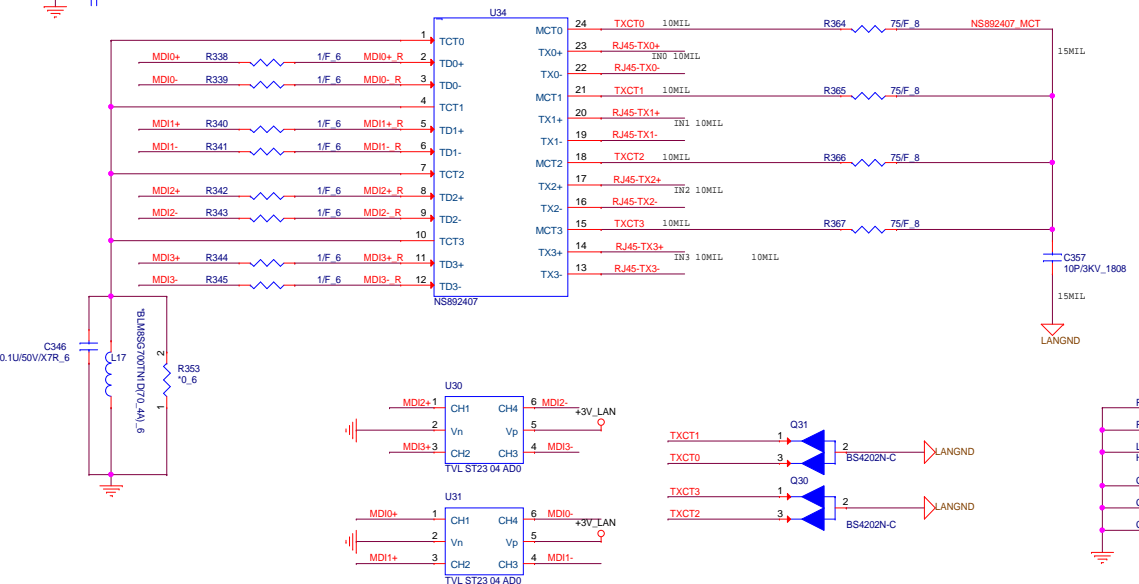
HeadPhone/Mic Combo Conn



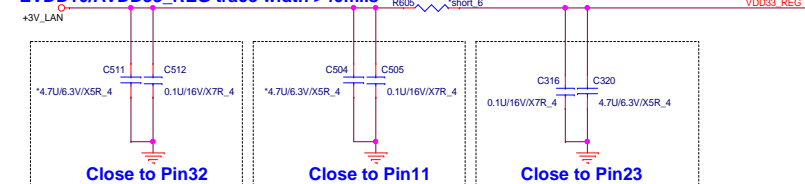
**R2248 value should be 2.49K (1%)
for all application.**



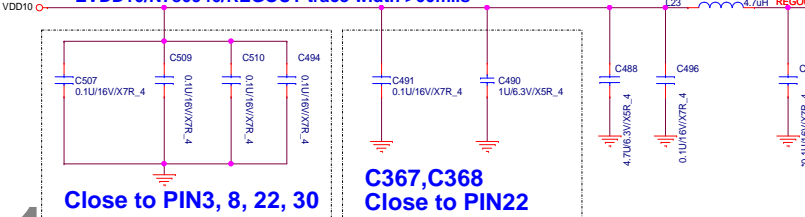
X'tal 25MHz



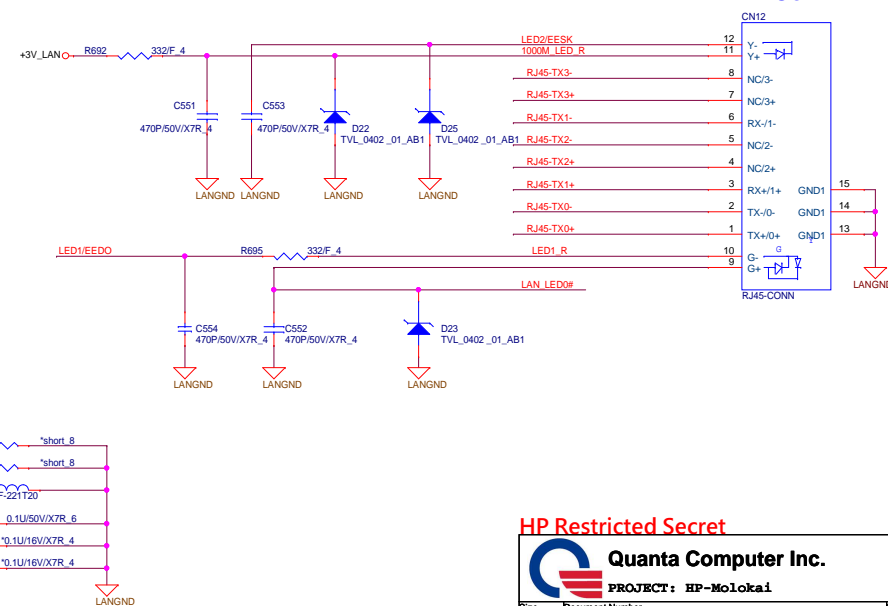
EVDD10/AVDD33_REG trace width >40mils



EVDD10/N780946/REGOUT trace width >60mils



LAN Conn



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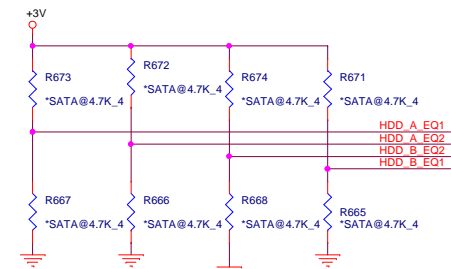
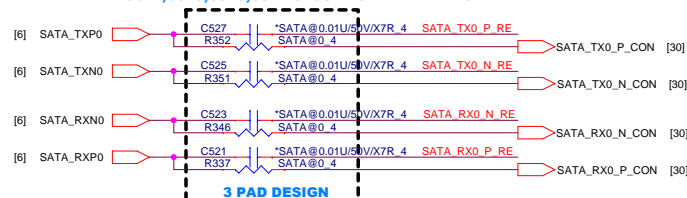
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PROJECT: HP-Molokai

Size Custom	Document Number RTL8161/RJ45	Rev 1A
Date: Monday, January 18, 2016	Sheet 27 of 54	

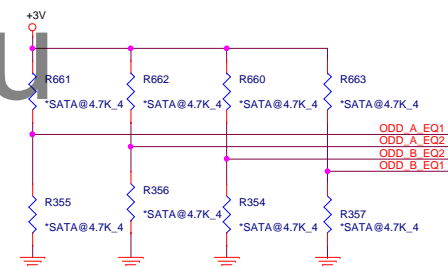
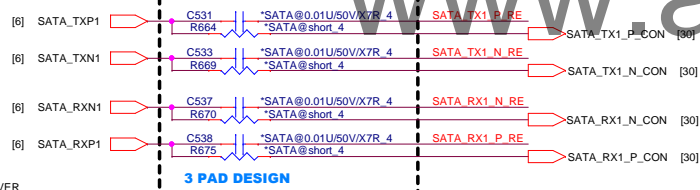
HDD REDRIVER

C521,C523,C525,C527 CLOSE TO RE-DRIVER IC

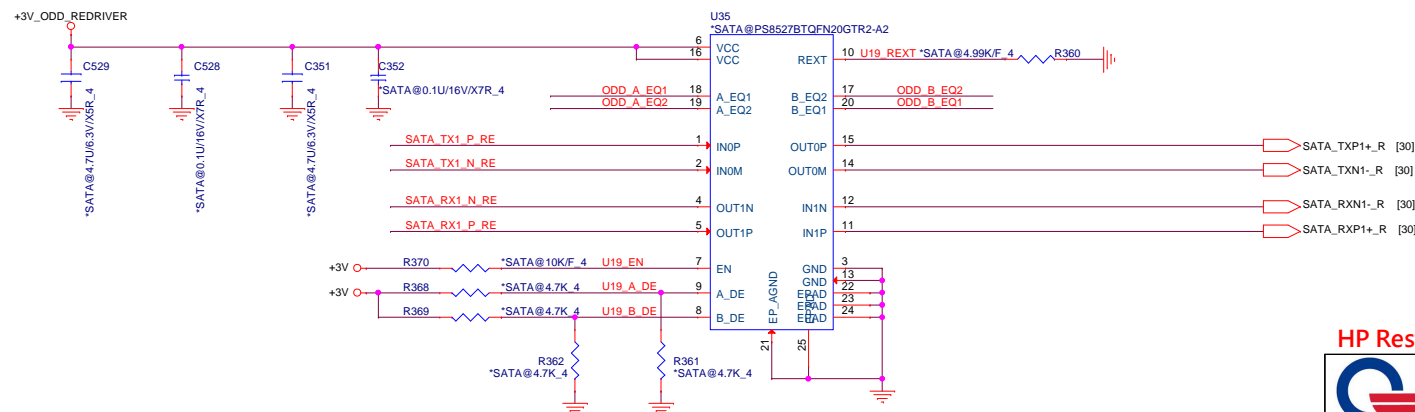


ODD REDRIVER

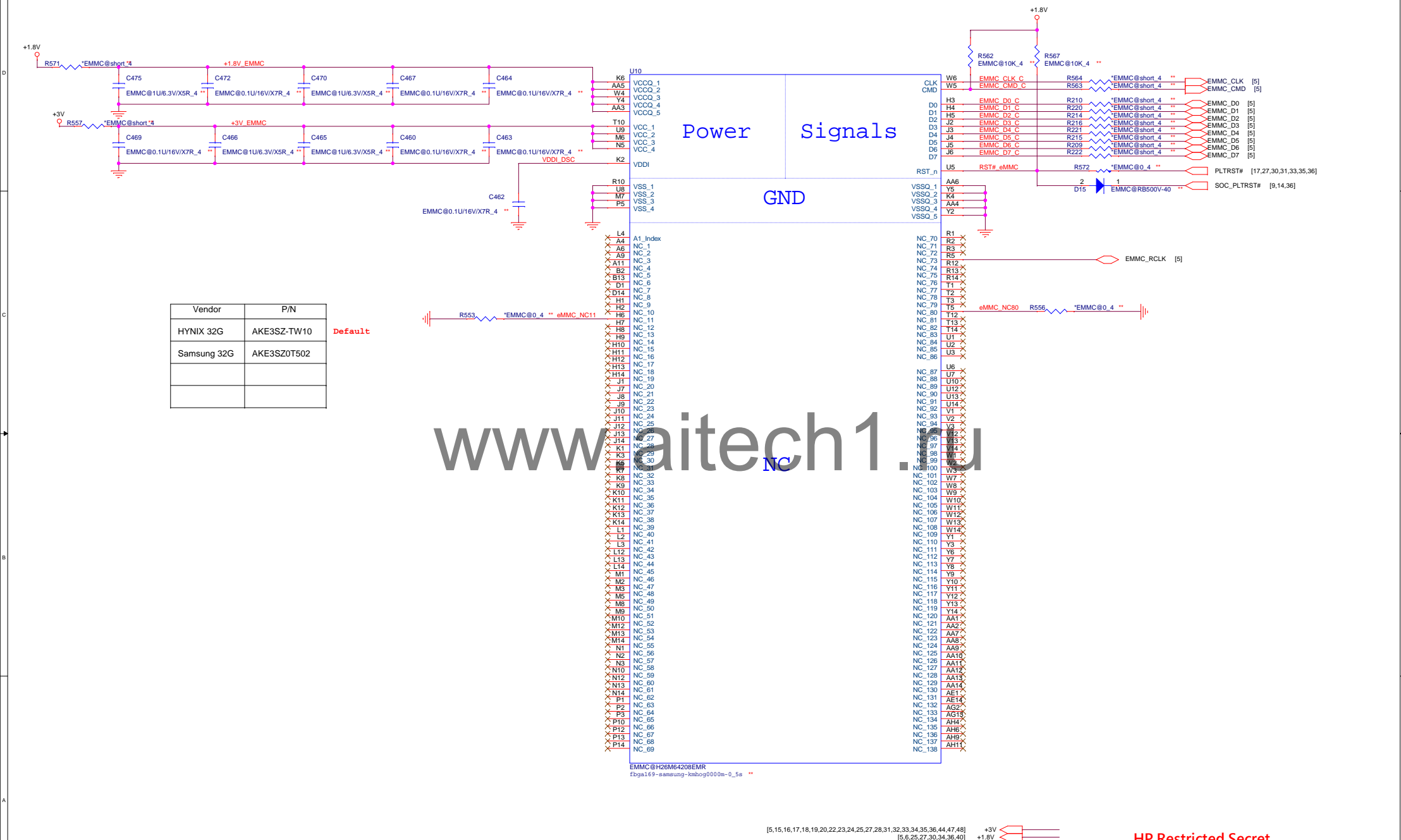
C531,C533,C537,C538 CLOSE TO RE-DRIVER IC



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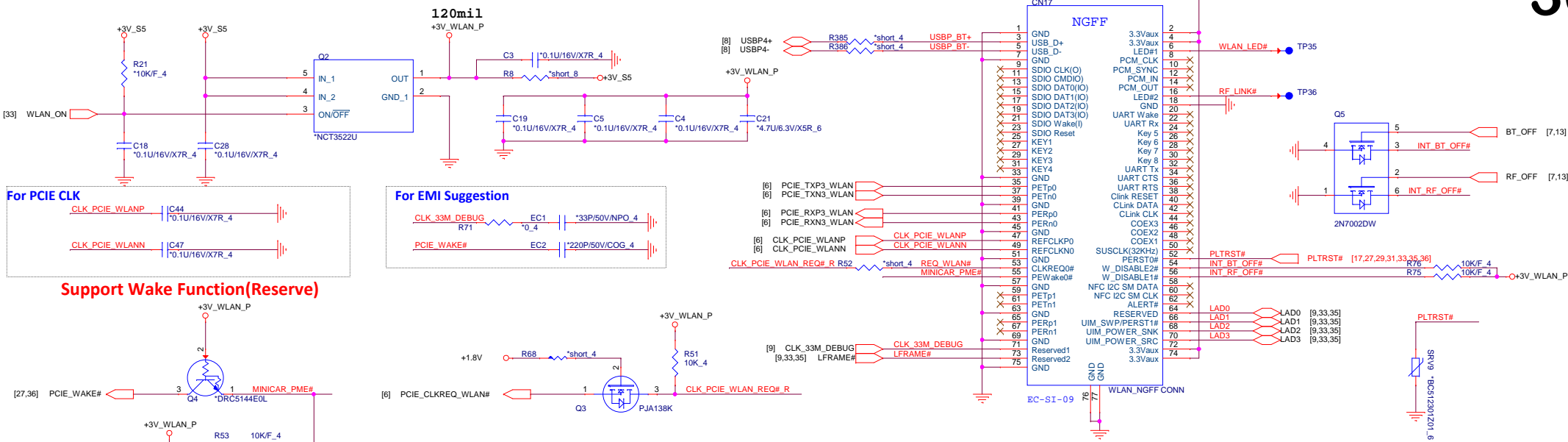
[5,15,16,17,18,19,20,22,23,24,25,27,28,31,32,33,34,35,36,44,47,48]
[5,6,25,27,30,34,36,40]

+3V
+1.8V

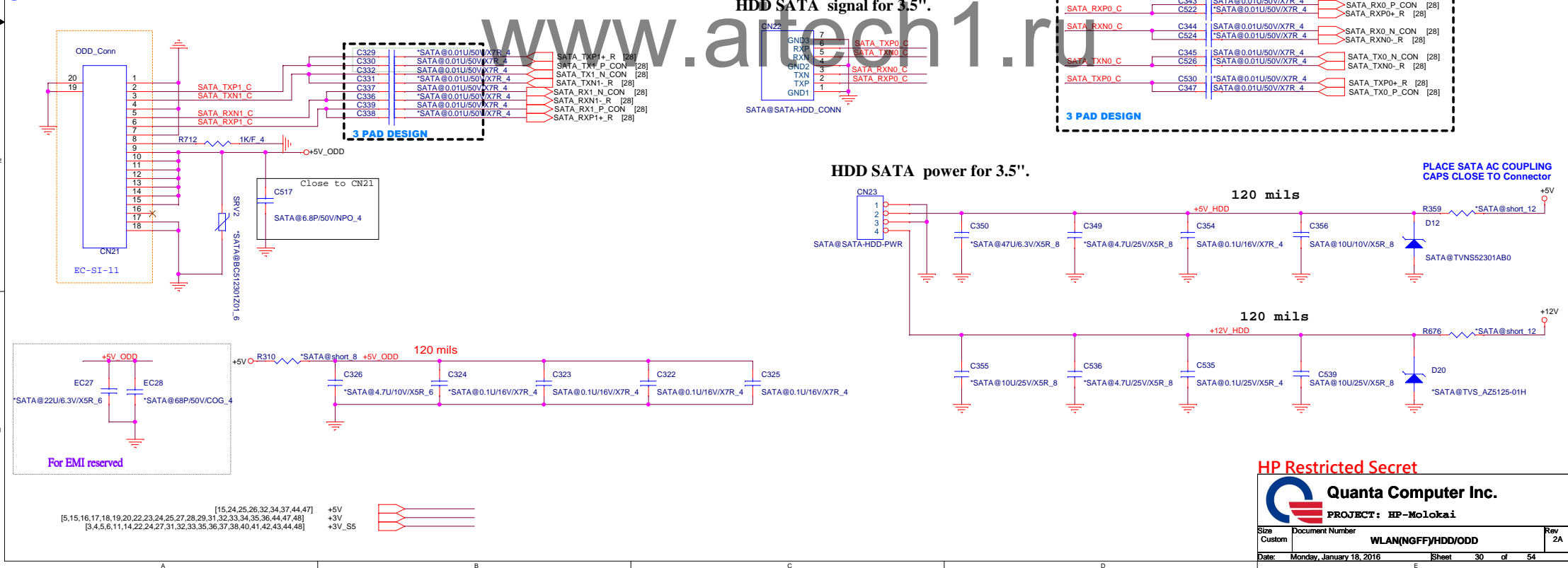
HP Restricted Secret

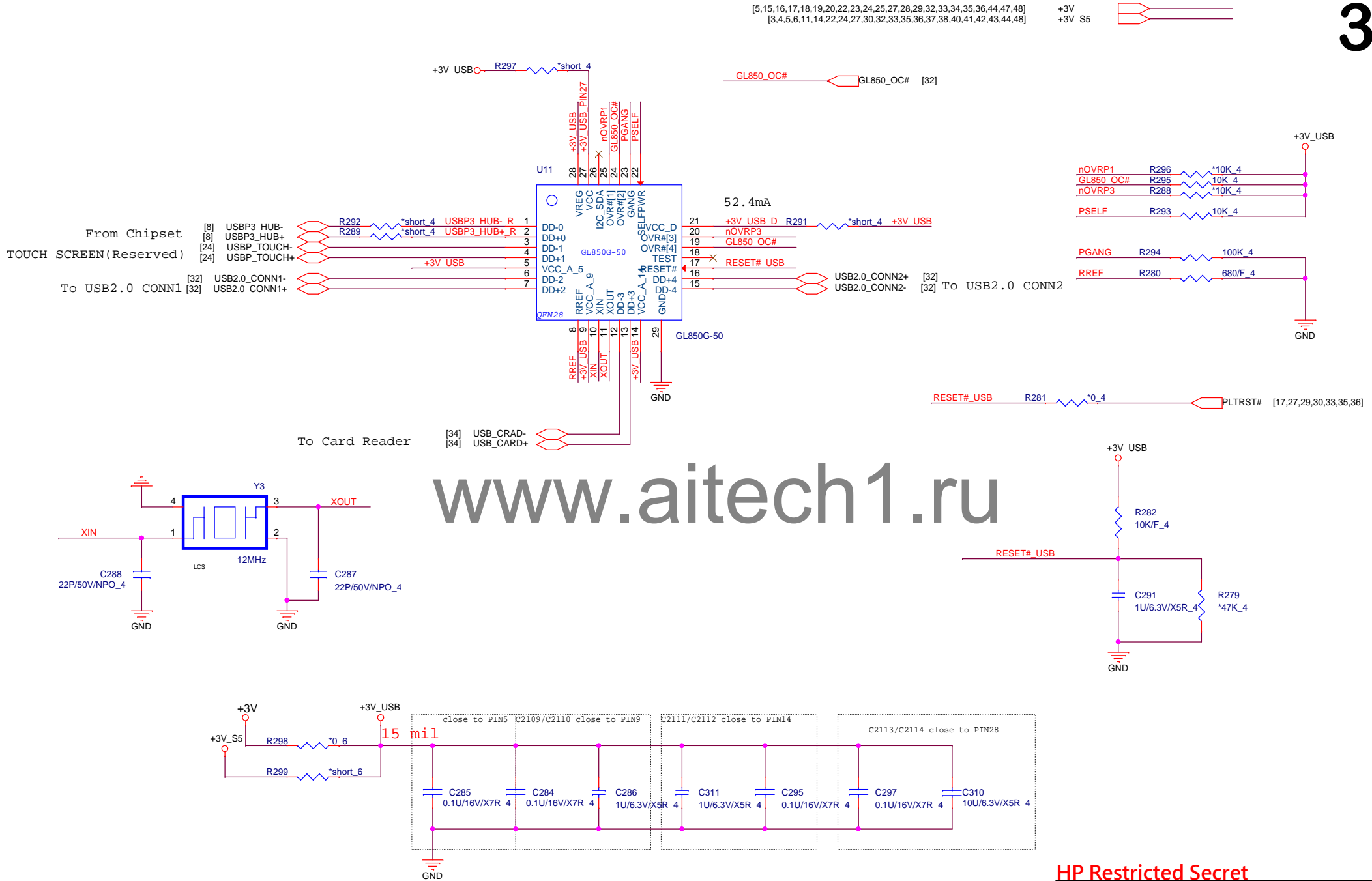
Quanta Computer Inc.
PROJECT: HP-Molokai

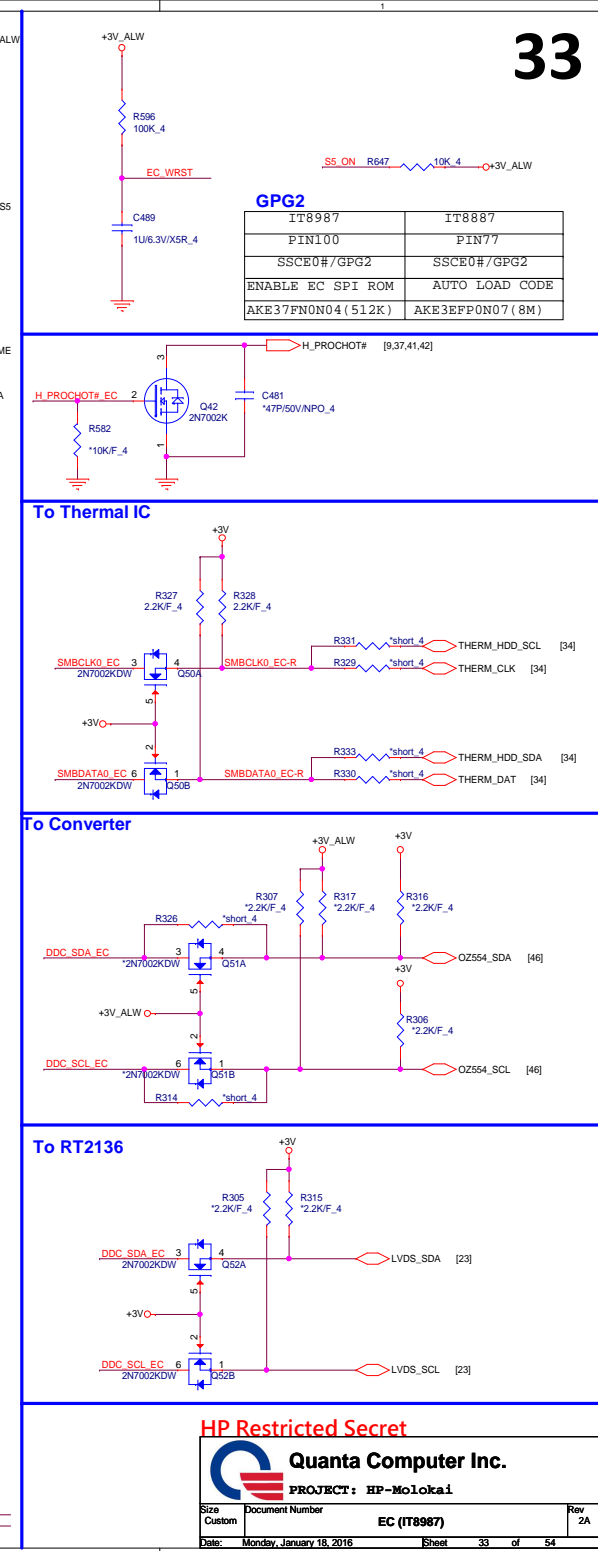
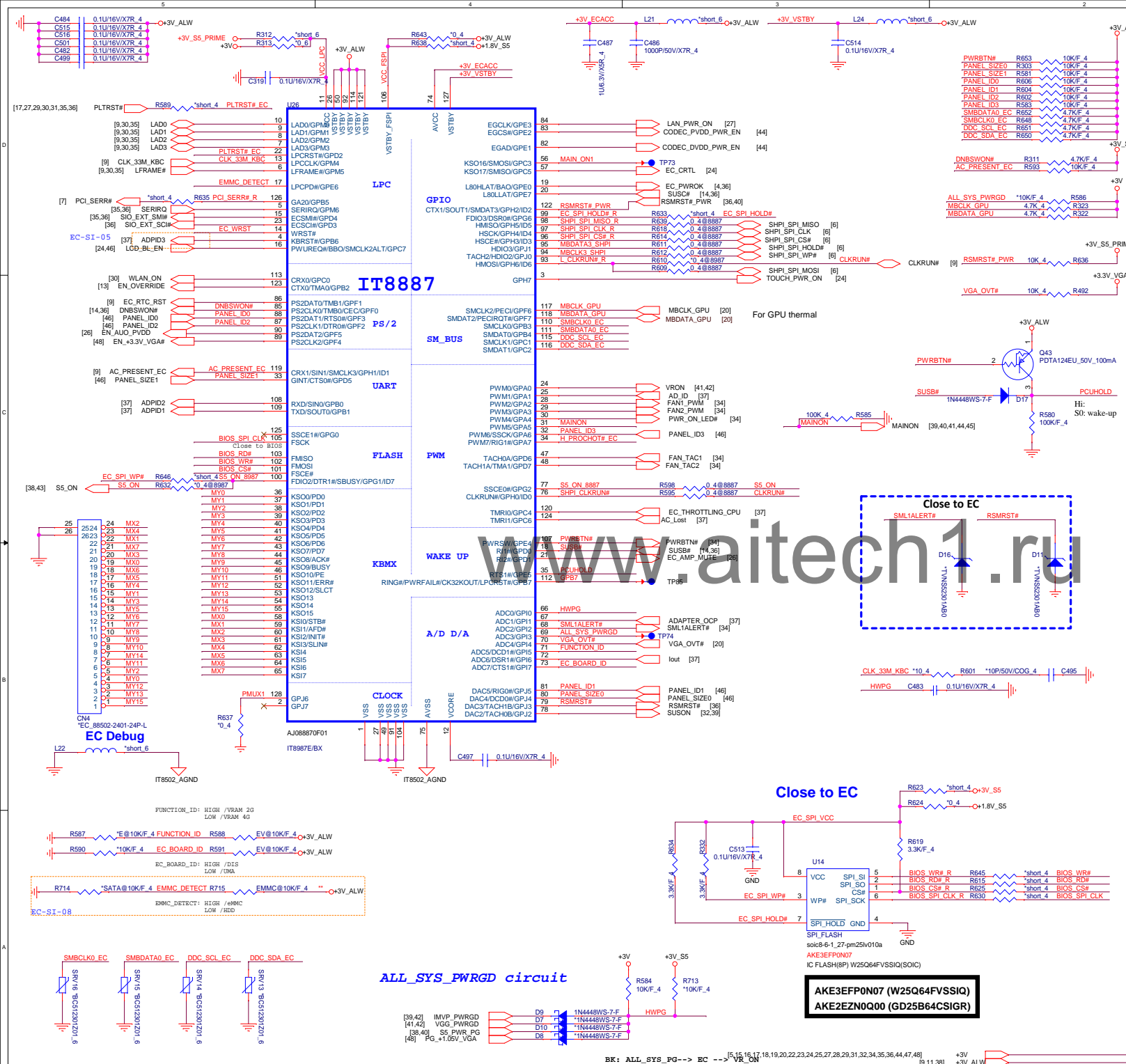
Size Custom Document Number eMMC Rev 1A
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Mini Card WLAN/BT(Optional)PCIe M.2_power(S5)

ODD



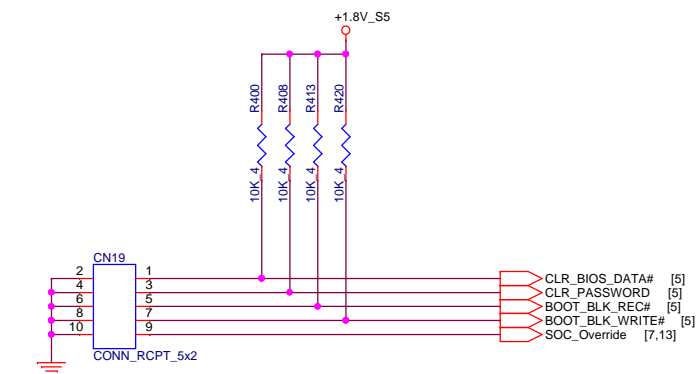




CLR_CMOS

Jumper	Pre-production	Production
BOOT_BLK_Recovery	X	X
BOOT_BLK_Enable	0	X

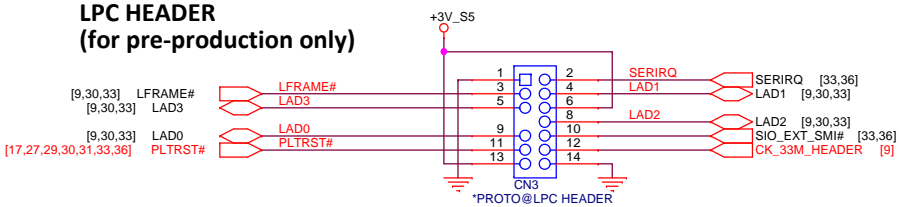
Jumper	Type
Pop	CLR_BIOS_DAT
Pop	CLR_PASSWD
Pop	BOOT_BLK_Recovery
Pop	BOOT_BLK_Enable



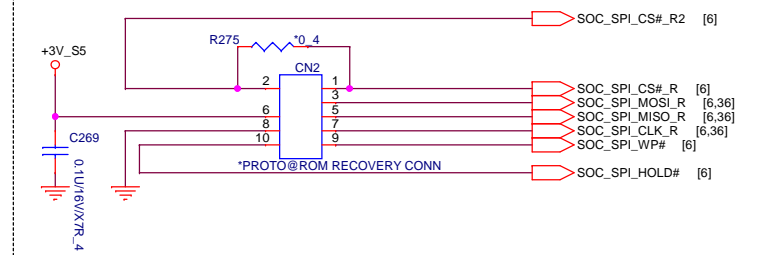
[3,4,5,6,11,14,22,24,27,30,31,32,33,36,37,38,40,41,42,43,44,48]
[5,6,7,8,9,11,13,14,22,33,36,40,41]
[5,15,16,17,18,19,20,22,23,24,25,27,28,29,31,32,33,34,36,44,47,48]



LPC HEADER (for pre-production only)

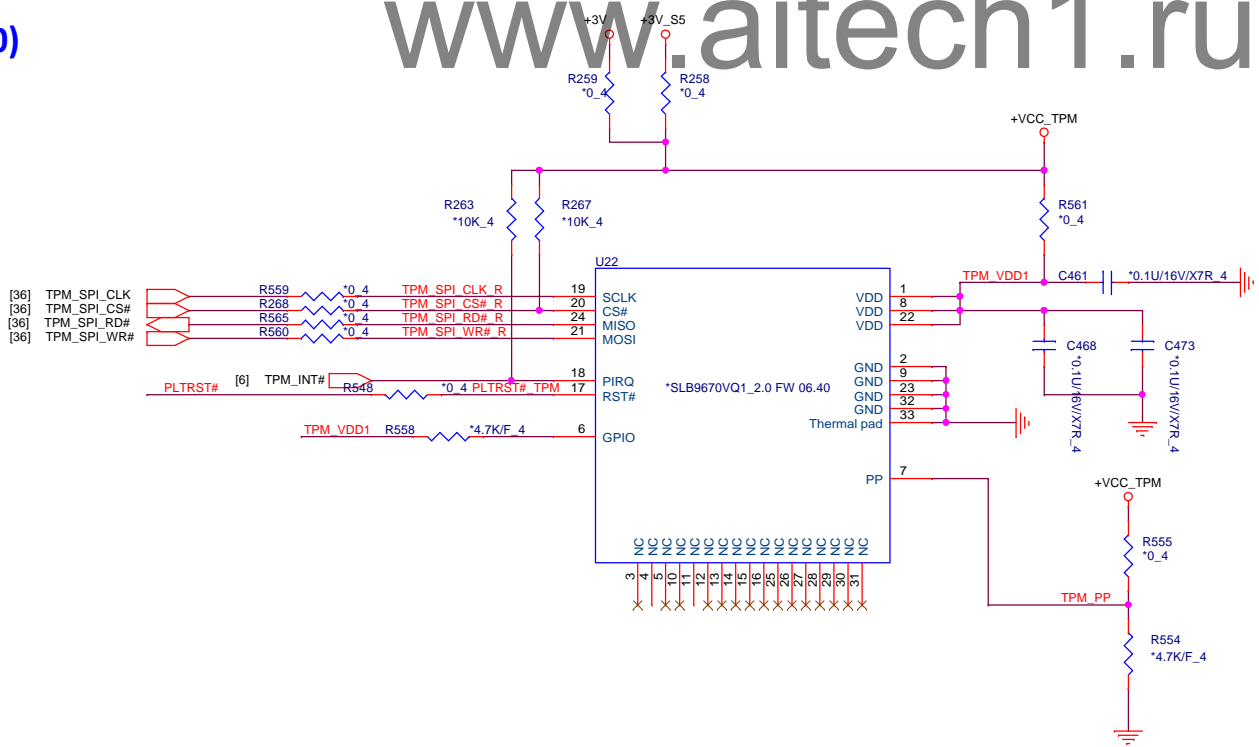


ROM recovery (for pre-production only)




TPM (1.2 or 2.0)

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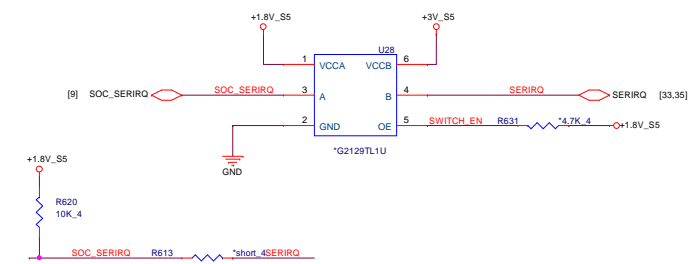


HP Restricted Secret

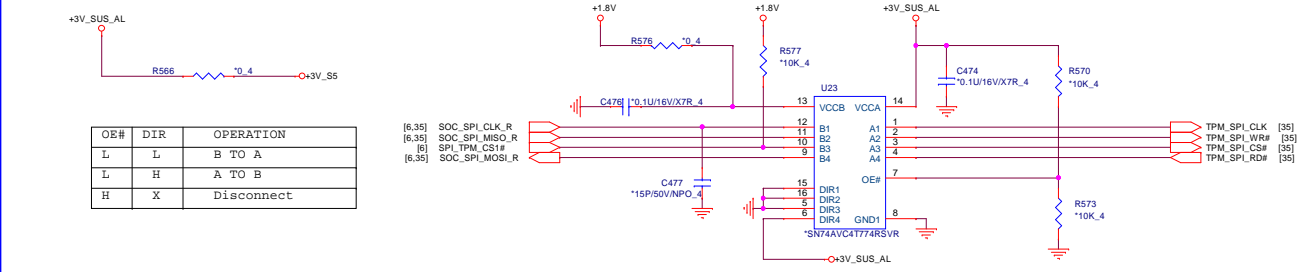
**Quanta Computer Inc.**
PROJECT: HP-Molokai

Size Custom	Document Number	JUMPER/LPCHeader	Rev 1A
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SERIRQ

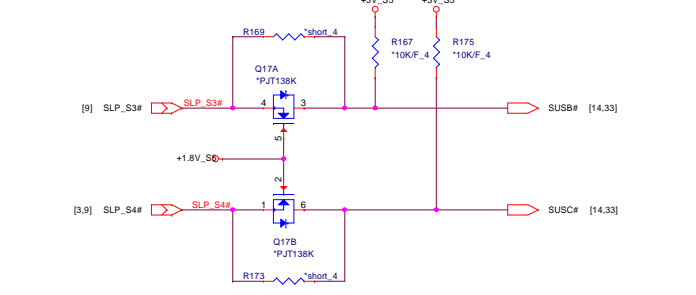


TPM level shift

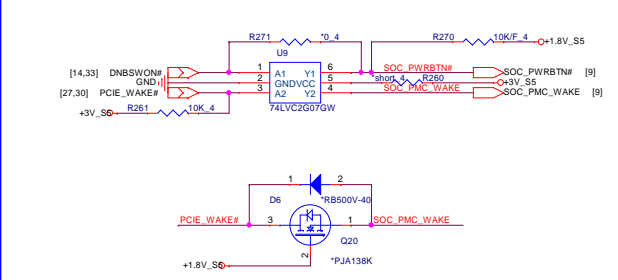


OE#	DIR	OPERATION
L	L	B TO A
L	H	A TO B
H	X	Disconnect

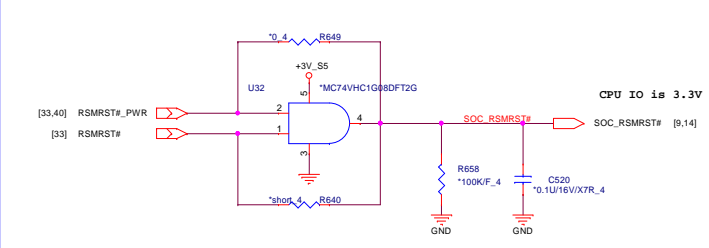
SUSB/C#



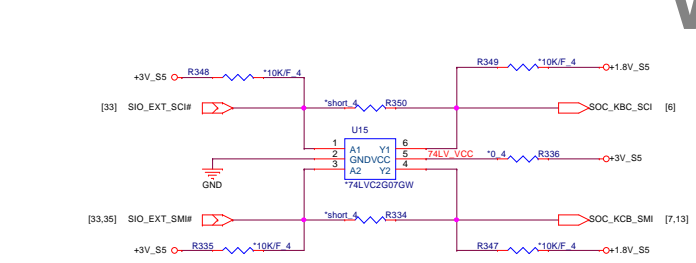
PWRBTN#/PCIE_WAKE#



RSMRST#



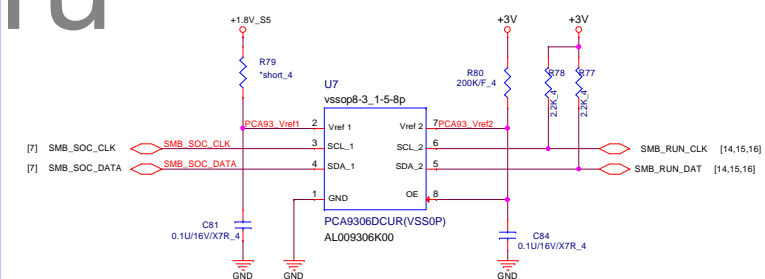
SCI#/SMI#



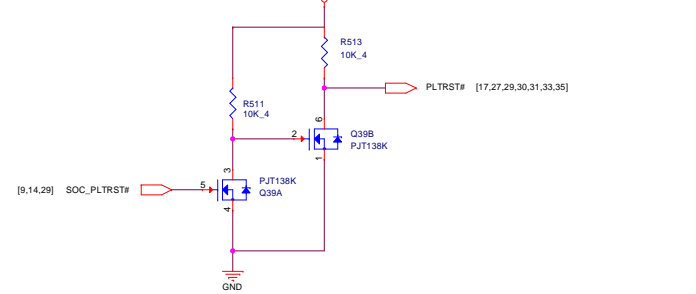
SYS_PWRGD

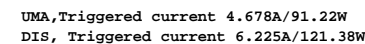


SO-DIMM/XDP SMBUS



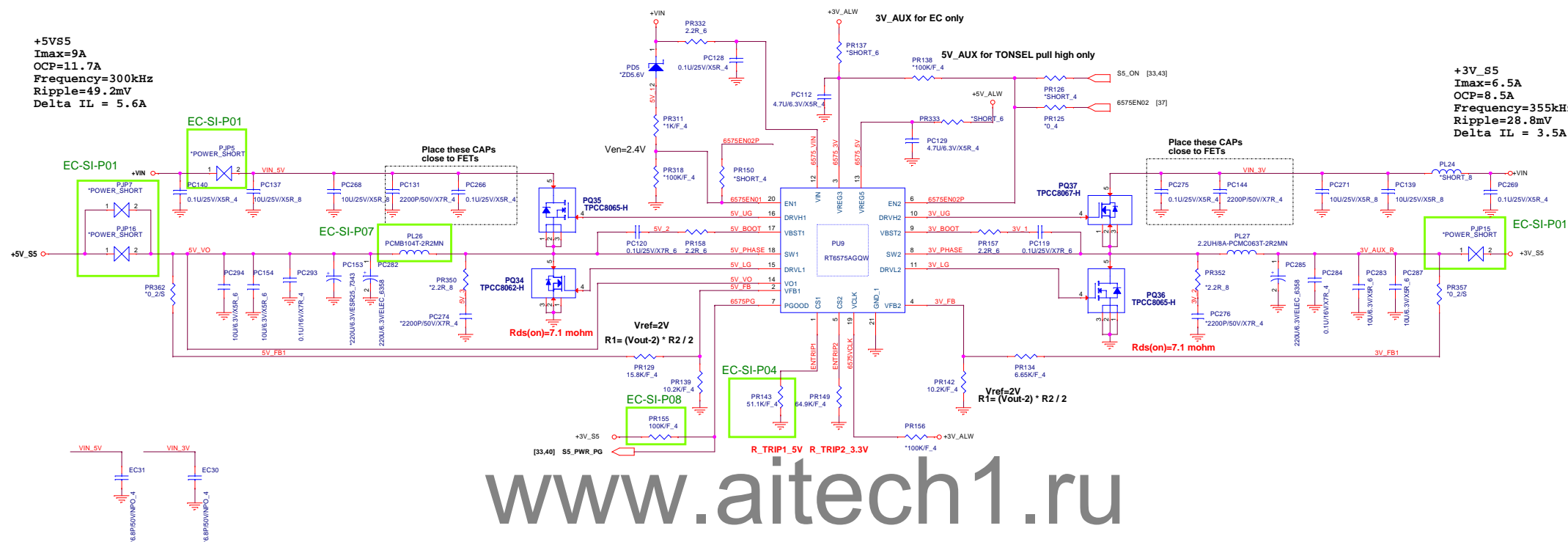
PLTRST#





+5VS5
 $I_{max}=9A$
 $OCP=11.7A$
 $Frequency=300kHz$
 $Ripple=49.2mV$
 $\Delta IL = 5.6A$

+3V_S5
 $I_{max}=6.5A$
 $OCP=8.5A$
 $Frequency=355kHz$
 $Ripple=28.8mV$
 $\Delta IL = 3.5A$




L/S Mosfet parameter

MOSFET	Package	ID (Ta=25C)	Rds_on_max
TPCC8067-H	DFN3x3	9A	26m
TPCC8062-H	DFN3x3	27A	7.1m

Power On sequencing

EN0	ENC	REF	VREG3	VREG5	SMPS1	SMPS2
LOW	LOW	OFF	OFF	OFF	OFF	OFF
> 2.4V	LOW	ON	ON	ON	OFF	OFF
> 2.4V	> 2.4V	ON	ON	ON	ON	ON

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PROJECT: HP-Molokai

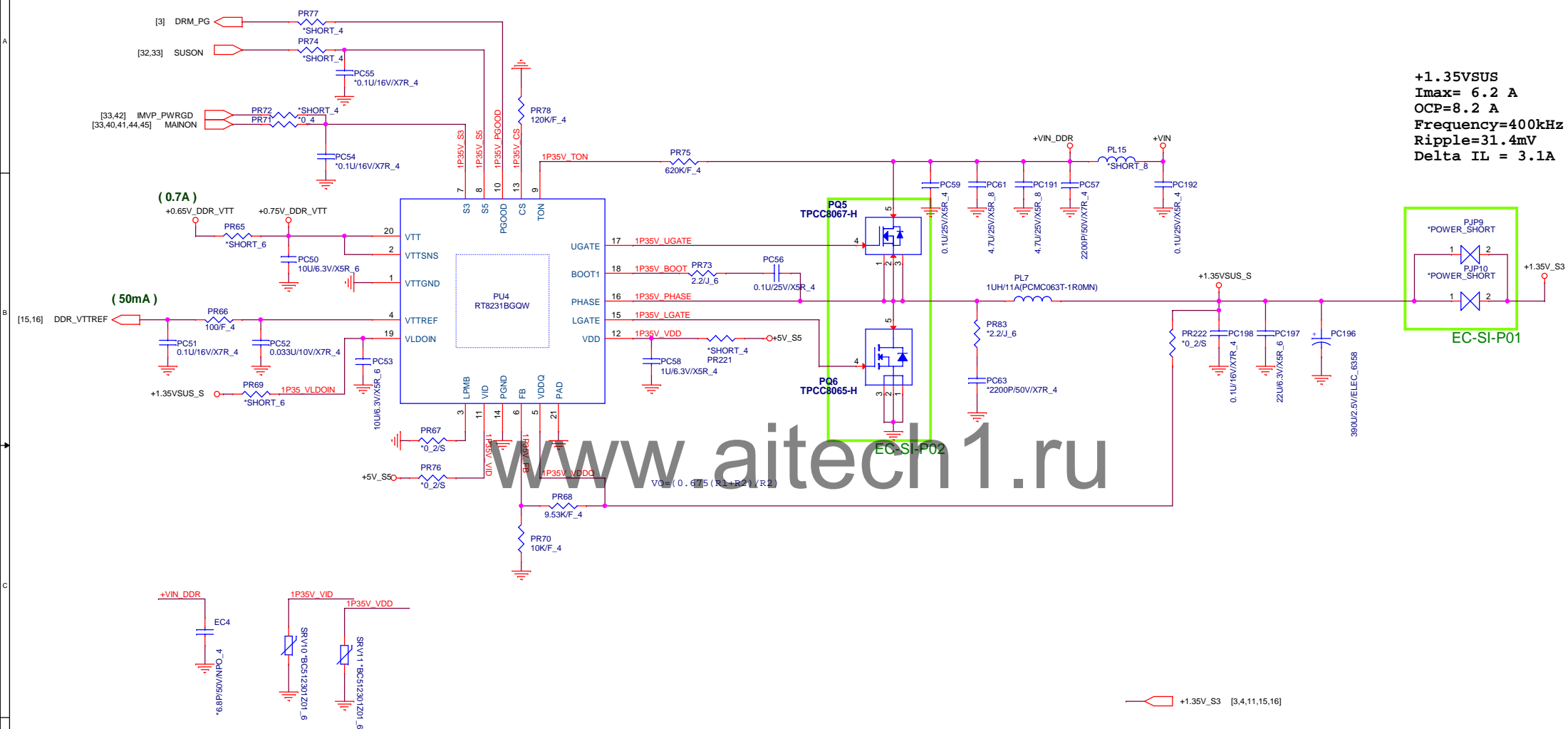
Size Custom	Document Number +3VS5/+5VS5(RT6575AGQW)	Rev 2
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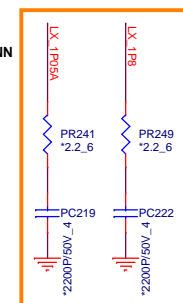
Quanta Computer Inc.

PROJECT: HP-Molokai



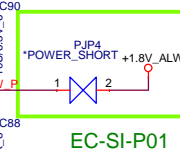
+3V_S5 [3,4,5,6,11,14,22,24,27,30,31,32,33,35,36,37,38,41,42,43,44,48]
 +1.8V_S5 [5,6,7,8,9,11,13,14,22,33,35,36,41]
 +3V_S5_PRIME [11,33]
 +1.5V [11,26]
 +1.24V_S5 [11]
 +1.15V_S5 [10]
 +5V_ALW [26,34,38]
 +1.05V_S5 [9,10,41,42]
 +1.8V [5,6,25,27,29,30,34,36]

+1.05VS5
 Imax= 2 A
 OCP=6 A
 Frequency=1.2MHz
 Ripple=5mV
 Delta IL = 1.3A

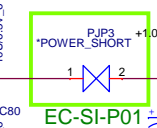


Snubber

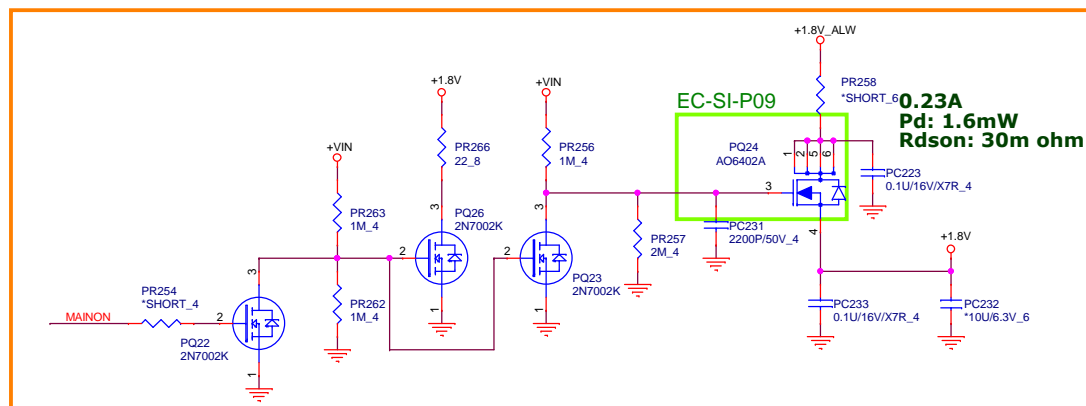
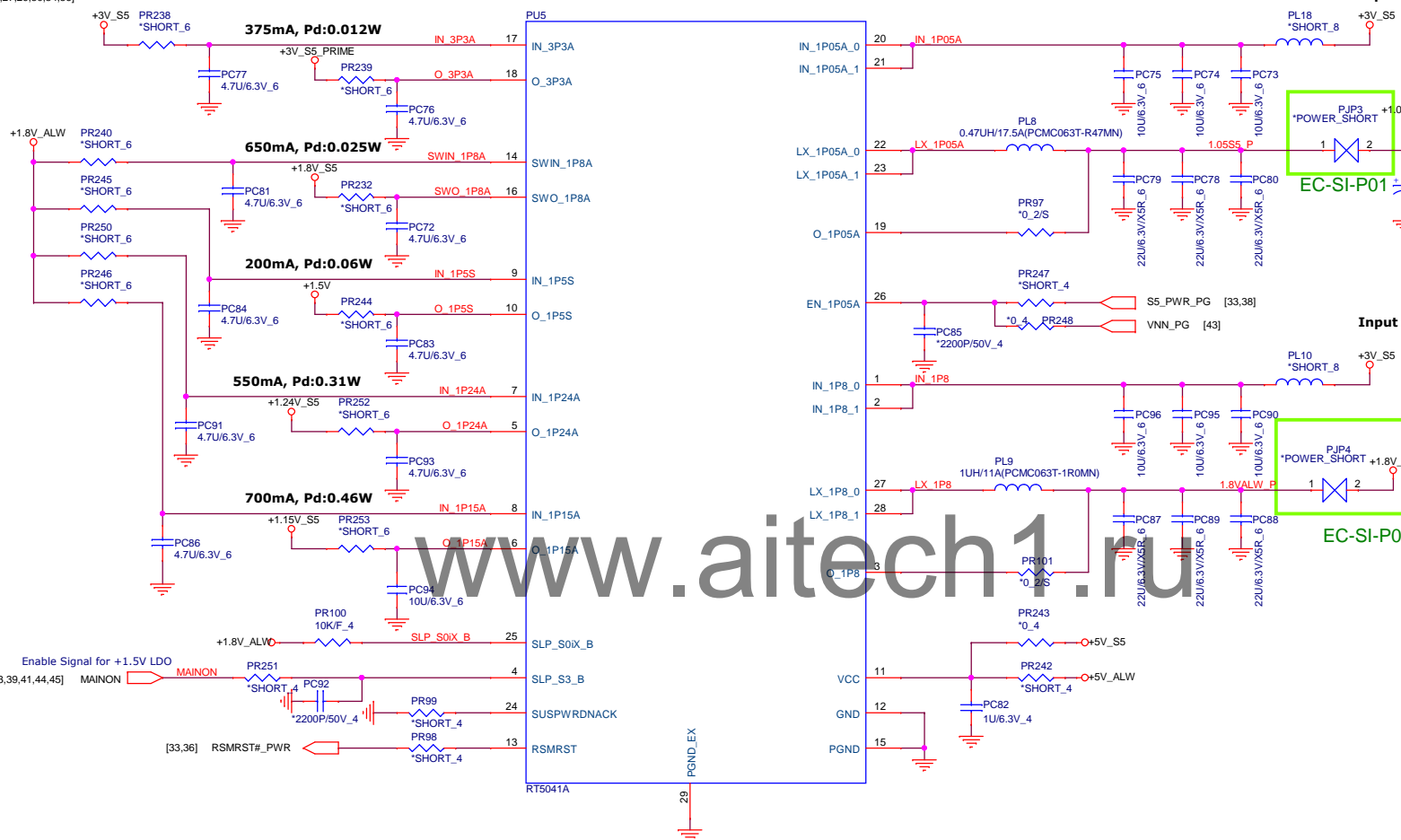
+1.8VALW
 Imax= 3.1 A
 OCP=6 A
 Frequency=1.2MHz
 Ripple=6.8mV
 Delta IL = 0.68 A



EC-SI-P01



EC-SI-P01

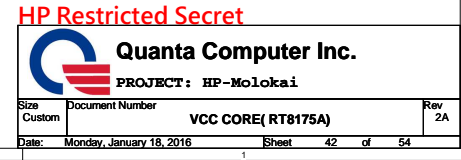


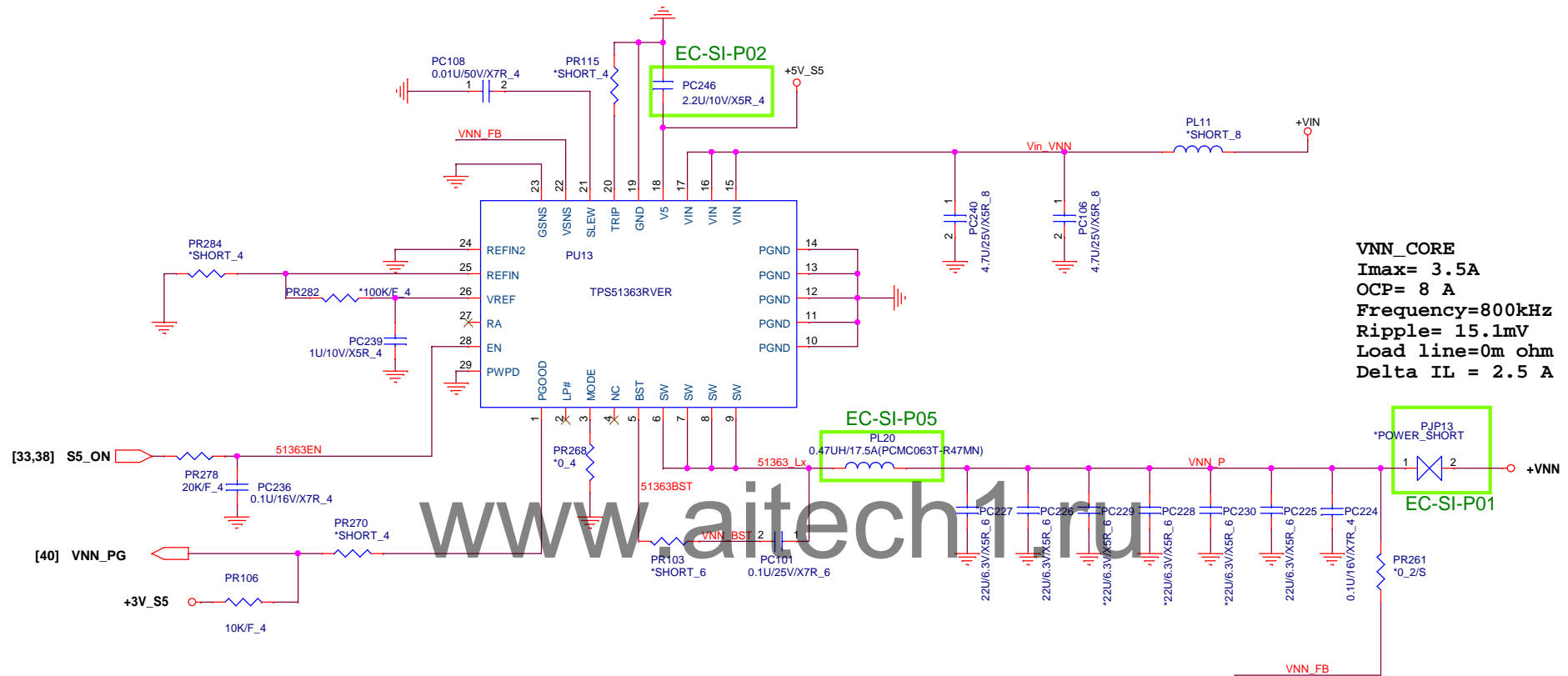
EC-SI-P09
 PQ24
 AO6402A
 0.23A
 Pd: 1.6mW
 Rdson: 30m ohm

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		MOIC (RT5041A)	
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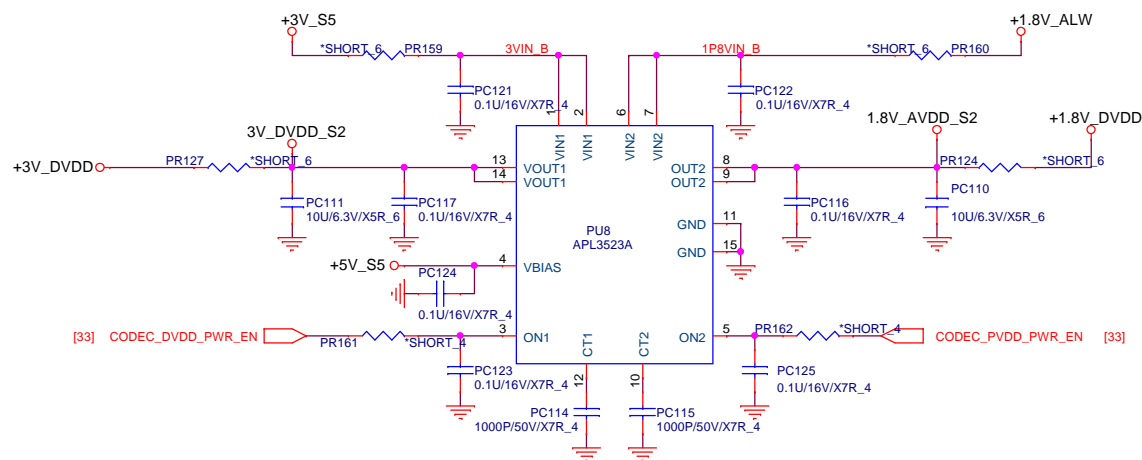
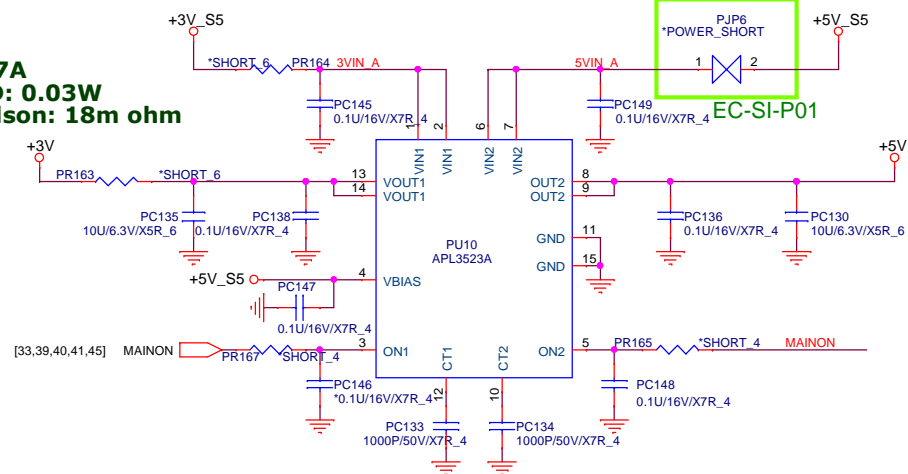
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1.7A
Pd: 0.03W
Rdson: 18m ohm

5.62A
Pd: 0.57W
Rdson: 18m ohm


0.5A
Pd: 0.01W
Rdson: 18m ohm

0.03A
Pd: 0.01W
Rdson: 18m ohm

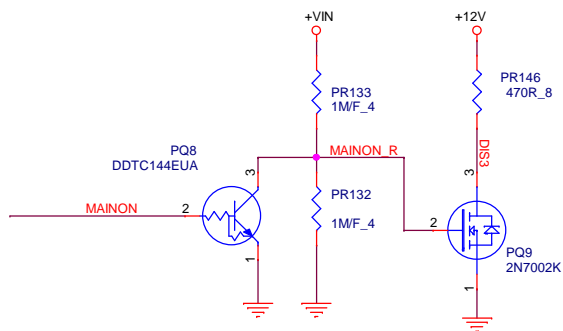
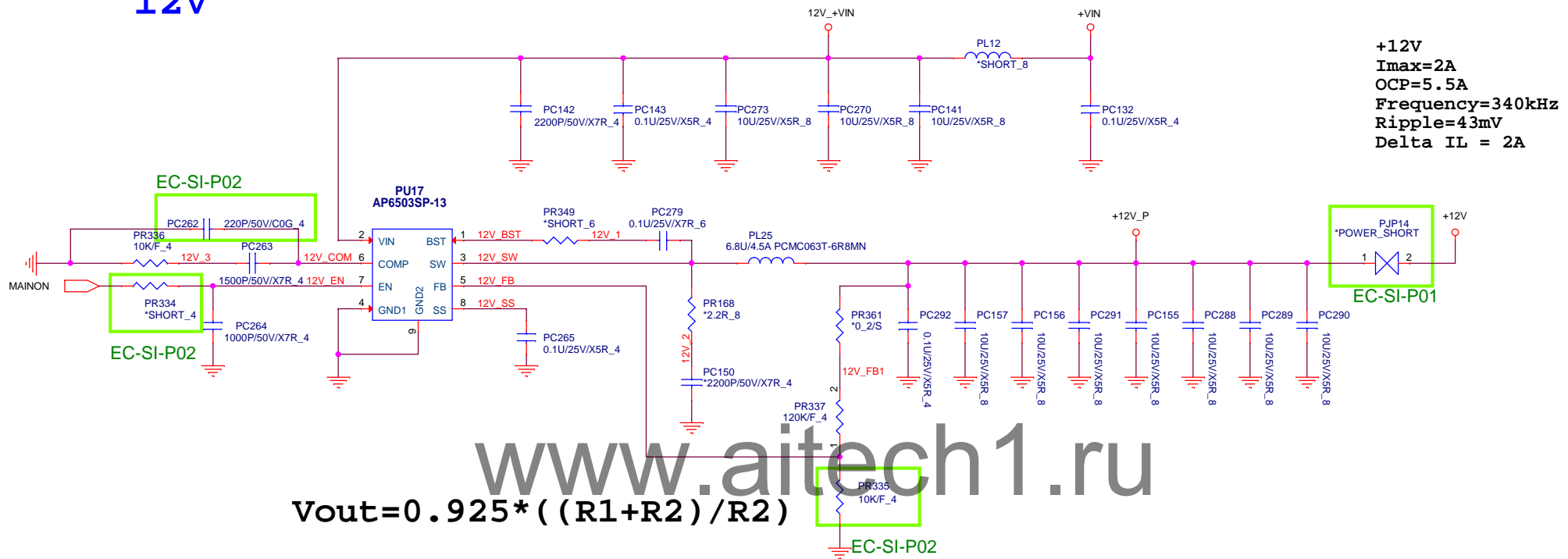


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 Quanta Computer Inc. PROJECT: HP-Molokai		Rev
		2A
Size	Document Number	
Custom		
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12V



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Quanta Computer Inc.

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PANEL Size[1:0]	Size
00	19.5/9.53"
01	21.5"
10	23.6"/23.8"
11	RESERVE

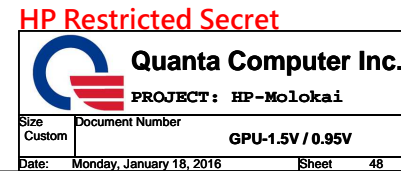
PANEL_ID[3:0]	Panel model
1111	No Connect
1110	INX M200HJJ-L20 FHD
1101	AUO M195RTN01.0 HD+
1100	LGD LM195WD1-TLA1 HD+
1010	Reserve

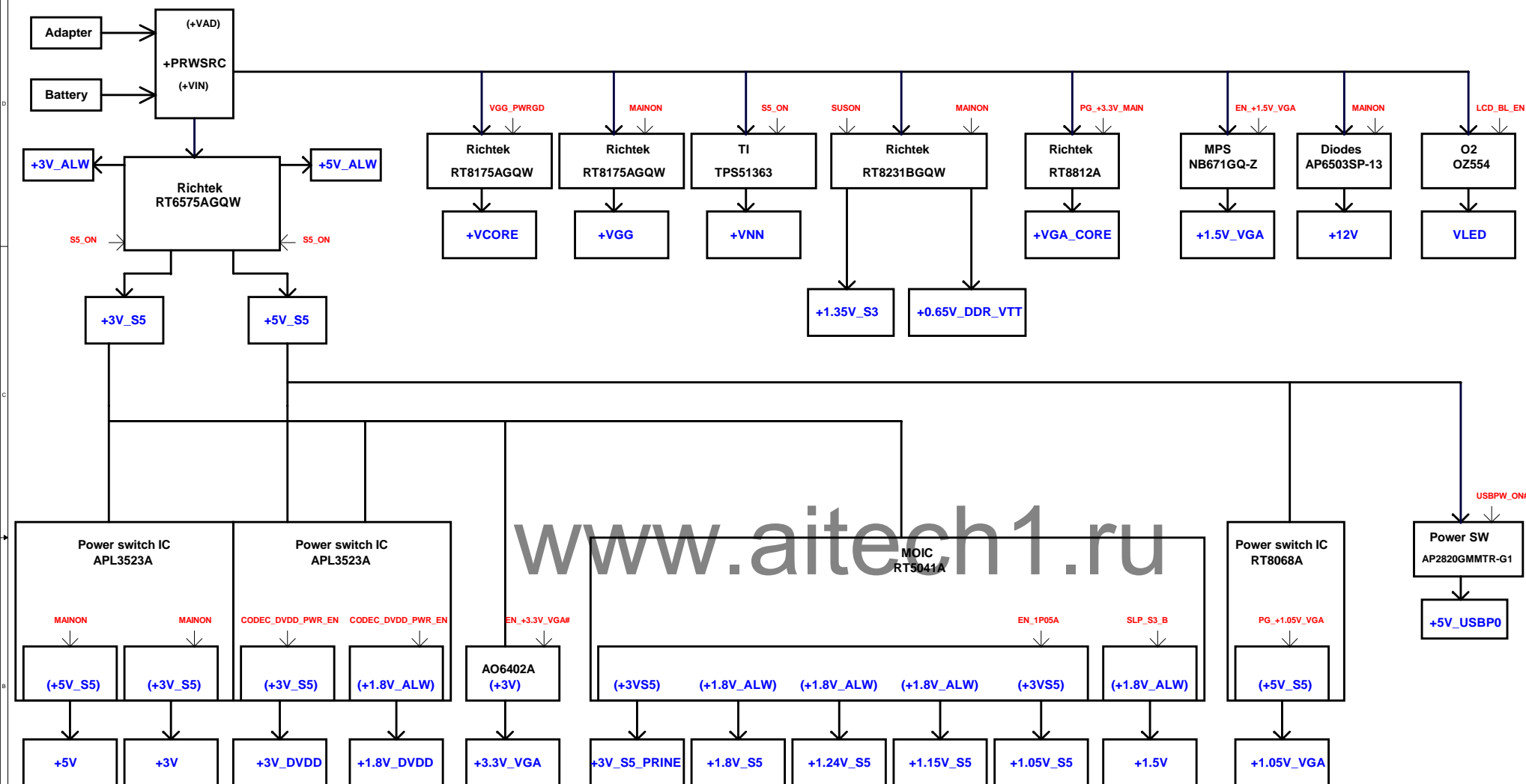
PANEL_ID[3:0]	Panel model
1111	No Connect
1110	INX M215HJK-L3B FHD eDP
1101	SDC LTM215HL01 FHD
1100	LGD LM215WF3-SLN1 FHD
1011	Reserve

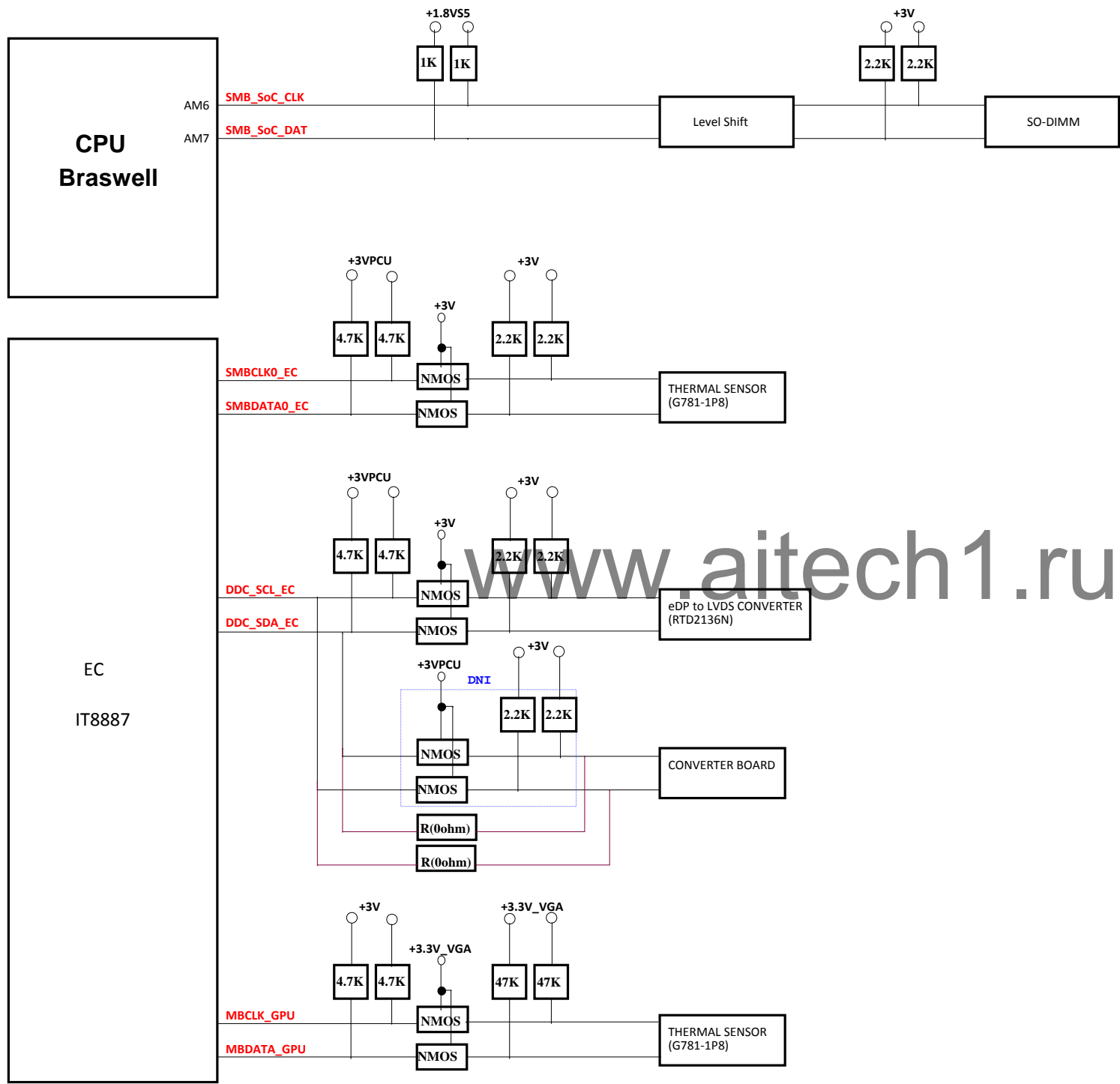
PANEL_ID[3:0]	Panel model
1111	No Connect
1110	INX M236HJK-L5B FHD eDP
1101	AUO M238HAN01.0 FHD
1100	LGD LM238WF1-SLE1 FHD
1011	SDC LTM238HL02 FHD
1010	Reserve

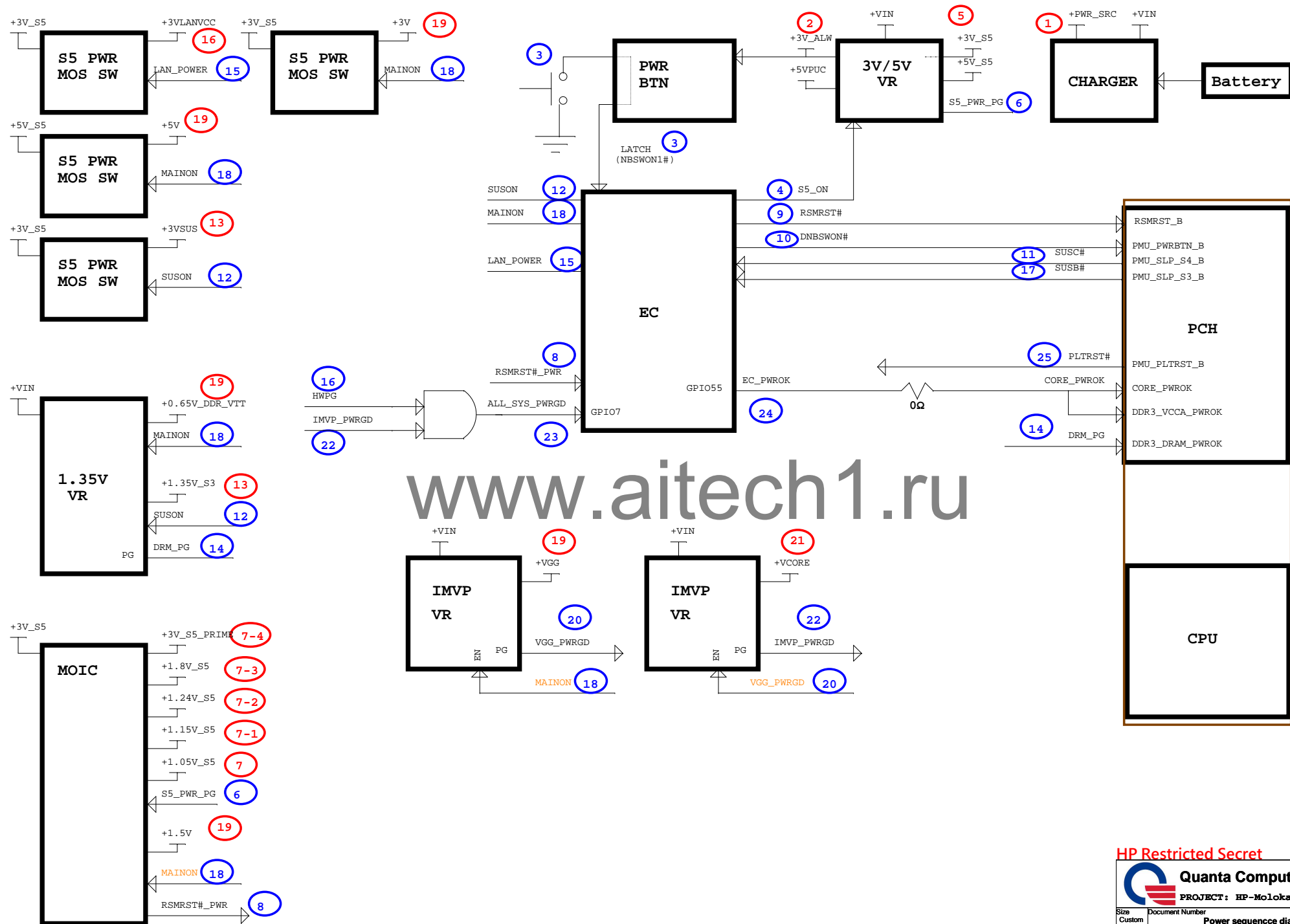
Panel_ID[3:0] = 1111 & Panel_Size[1:0] = 11 is reserved for cabling detection by "No connection".

48



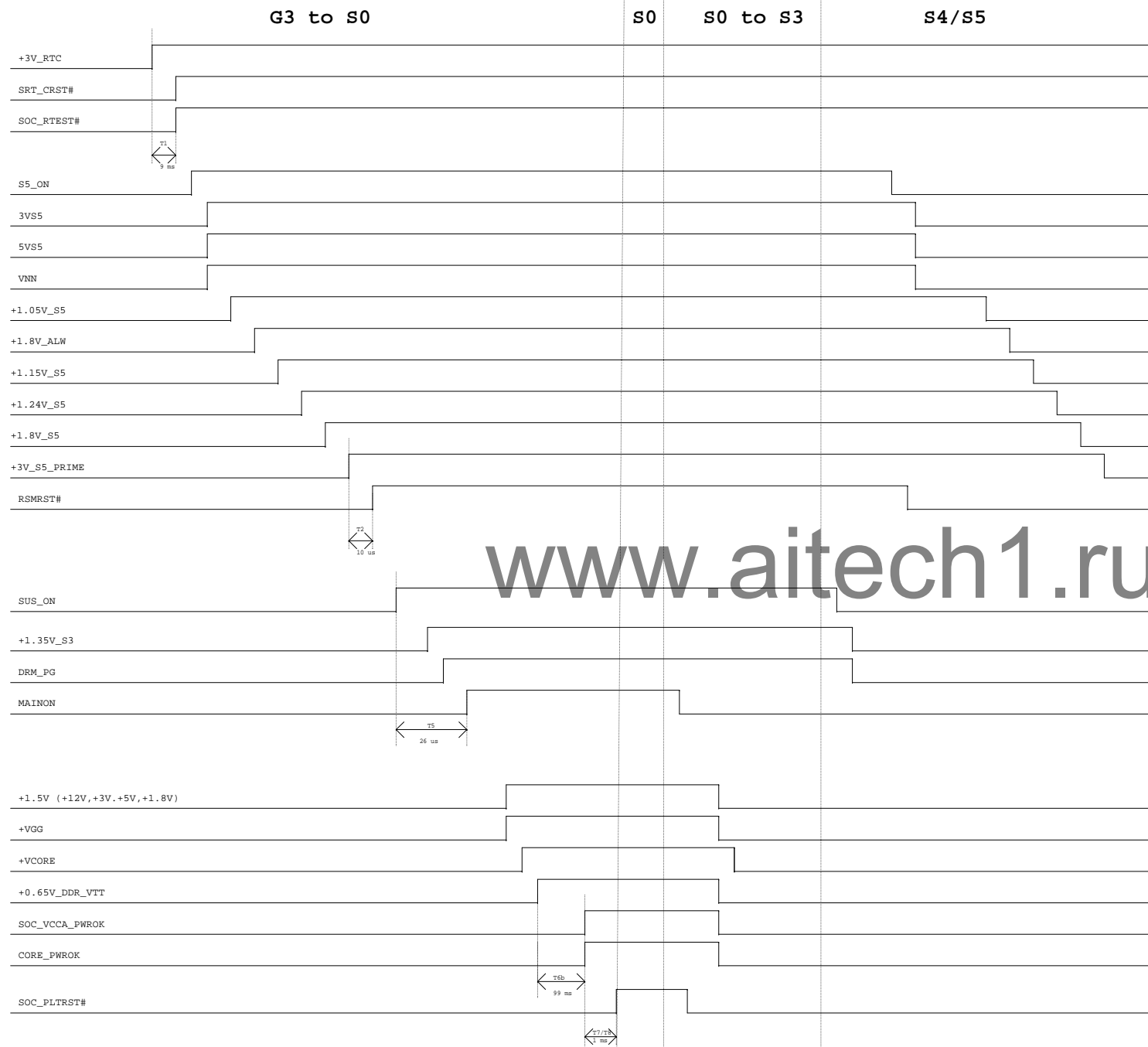




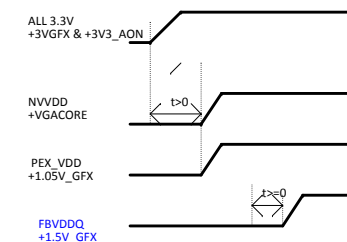


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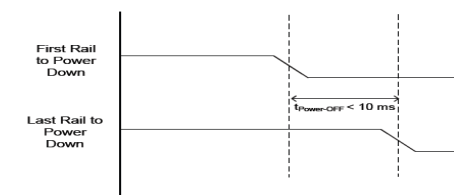
HP Restricted Secret



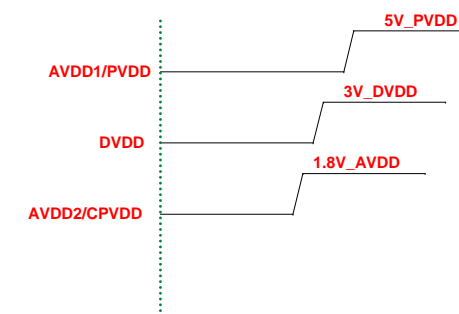
N16V Power up sequence



N16V Power down sequence



AUDIO POWER SEQUENCE



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N91A EE Schematic EC Tracking Record DB to SI version

EC #	Page	Description	Part Affected
EC-SI-01	32	add GND PAD for EMI	H20,H21
EC-SI-02	26	change Audio speaker connector from 1 4pin to 2 2pin	CN25,CN26
EC-SI-03	07	change board ID for SI stage, R537 no stuff, R544 stuff	R537,R544
EC-SI-04	34	add second fan function	CN27,R709,C574,EC58,EC59,R710,R711,C575
EC-SI-05	33	add ADPID3 for smart adapter	U26.pin4,PQ38,PR295
EC-SI-06	15	add EC60 for EMI	EC60
EC-SI-07	20	remove R483 double pull high for PSI	R483
EC-SI-08	33	add EMMC_DETECTfunction for EC check sku	R714,R715
EC-SI-09	30	change CN17 footprint	CN17
EC-SI-10	24,34	change D4,SU1,D21,D24,D26 to stuff for ESD	D4,SU1,D21,D24,D26
EC-SI-11	30	Change ODD connector to 18 pin	CN21
EC-SI-12	34	Change connector to FFC type of card reader daughter board	CN24
EC-SI-12	26	change AL6/AL7/AL9/AL10 to 0 ohm for Realtek suggestion	AL6,AL7,AL9,AL10

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N91A Power Schematic EC Tracking Record DB to SI version

EC #	Page	Description	Part Affected
EC-SI-P01	38~48	Change default open to default short	PJP1~PJP11, PJP13~16
EC-SI-P02	39,43,45,46,48	Downsize components	PC246, PR334, PR335, PC262, PC14, PC174, PQ5, PQ6 PC21, PC181, PC6
EC-SI-P03	47, 48	Correct connection	
EC-SI-P04	38,47	Fine tune OCP function	PR143, PR86
EC-SI-P05	43,47	Change choke for transient	PL17, PL20
EC-SI-P06	48	Fine tune offset voltage	PR21
EC-SI-P07	38, 47	Change components for ripple voltage	PL26, PC65
EC-SI-P08	42	Change components CPU 6.5W	PQ4, PR16, PR46, PR198, PR199
EC-SI-P09	40,47,48	Change components for common part using	PQ24, PR227, PR231, PQ12, PQ14, PQ16
EC-SI-P10	47	Fine tune soft start	PR90, PC208
EC-SI-P11	43	Reducing VGG Ring Voltage	PR290, PR267, PC234
EC-SI-P12	37	Add components for SMART ID function	PR281, PR300, PR295, PR291, PR310, PR271, PR285, PR407 PQ29, PQ31, PQ38

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